MT6573 HSPA Smartphone Application Processor Technical Brief

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Revision History

Revision	Date	Comments
0.1	Dec 17, 2010	Draft Version.
0.1b	Dec 22, 2010	Modify pin MUX section according to SA's suggestions.
0.1c	Dec 27, 2010	Correct and add power domain description for GPIO.
0.2	Jan 3, 2011	Correct ball name and EMI related signal. Add IO electrical characteristics.
0.3	Jan 7, 2011	Correct analog pin description and power domain.
0.3a	Jan 11, 2011	Correct SIM2 I/F description in pin MUX table.
0.3b	Jan 17, 2011	Correct PMU/Analog pin descriptions.
0.3c	Jan 25, 2011	Correct IO electrical characteristics.
0.4	Mar 3, 2011	Update MPEG4 video specification to FWVGA. Update PMU power electrical characteristics.
0.4a	Mar 15, 2011	Update pin MUX table Update IO electrical characteristics table
0.5	June 23, 2011	Update MIPI electrical characteristics Update buck converter datasheet

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TABLE OF CONTENTS

Revision History 2

Preface 4

1 System Overview 5
- 1.1 General Description 5
- 1.2 Platform Features 7
- 1.3 MODEM Features 9
- 1.4 Multimedia Features 10

2 Product Description 11
- 2.1 Pin Description 11
- 2.2 Electrical Characteristics 67
- 2.3 System Configuration 75
- 2.4 Power on Sequence 76
- 2.5 Analog Baseband 78
- 2.6 Power Management Unit 95
- 2.7 Package Information 110
- 2.8 Ordering Information 112

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Preface

Acronym for Register Type

R/W	Capable of both read and write access
RO	Read only
RC	Read only. After reading the register bank, each bit which is HIGH(1) will be cleared to LOW(0) automatically.
WO	Write only
W1S	Write only. When writing data bits to register bank, each bit which is HIGH(1) will cause the corresponding bit to be set to 1. Data bits which are LOW(0) has no effect on the corresponding bit.
W1C	Write only. When writing data bits to register bank, each bit which is HIGH(1) will cause the corresponding bit to be cleared to 0. Data bits which are LOW(0) has no effect on the corresponding bit.

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1 System Overview

1.1 General Description

MT6573 is a highly integrated 3.75G baseband system-on-chip (SOC) platform which incorporates advanced features like HSPA R6 modem, 676MHz ARM11 CPU, OpenGL ES 2.0 3D graphics, 8M camera ISP, Programmable hardware video codec, and FWVGA (854x480) display. MT6573 can help phone manufacturers build high performance 3.75G smart phone with PC-like browser, 3D gaming, and cinema class home entertainment experience.

The chip integrates two ARM1176 MCUs and a powerful Dual MAC DSP processor with advanced system power management and multimedia capabilities. MT6573 interfaces to NAND flash memory and 32-bit LPDDR for optimal performance, while supporting booting from NAND to minimize overall BOM cost. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays, MMC/SD cards, and external Bluetooth, WiLAN, and GPS modules.

The Application Processor, an ARM1176JZFS which include a Vector Floating Point Coprocessor, offers the processing power necessary to support the latest OpenOS along with its demanding applications such as Web Browsing, Email, GPS Navigation, and Games. All while viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D Graphics OpenGL ES 2.0 acceleration. The MFlexVideo programmable multi-standard codec and an advanced audio subsystem are included to provide advanced multimedia applications and services such as Streaming audio and video, a multitude of decoders and encoders such as H.264 and MPEG-4. To enrich camera feature, MT6573 equips an 8M camera ISP with advanced features like auto focus, anti-handshake, continuous video AF, face detection, burst shot, optical zoom, panorama view and 3D photo. Other audio support includes FR, EFR, HR, and AMR vocoders, polyphonic ringtones, and advanced audio functions such as echo cancellation, hands-free speakerphone operation, and noise cancellation.

Modem subsystem built by An ARM1176JZS core, Dual MAC DSP, and EDGE/GPRS and HSPA coprocessors offers powerful capability to support Category 8 (7.2 Mbps) HSDPA downlink and Category 6 (5.76 Mbps) HSUPA uplink data rates, as well as Class 12 GPRS and EDGE.

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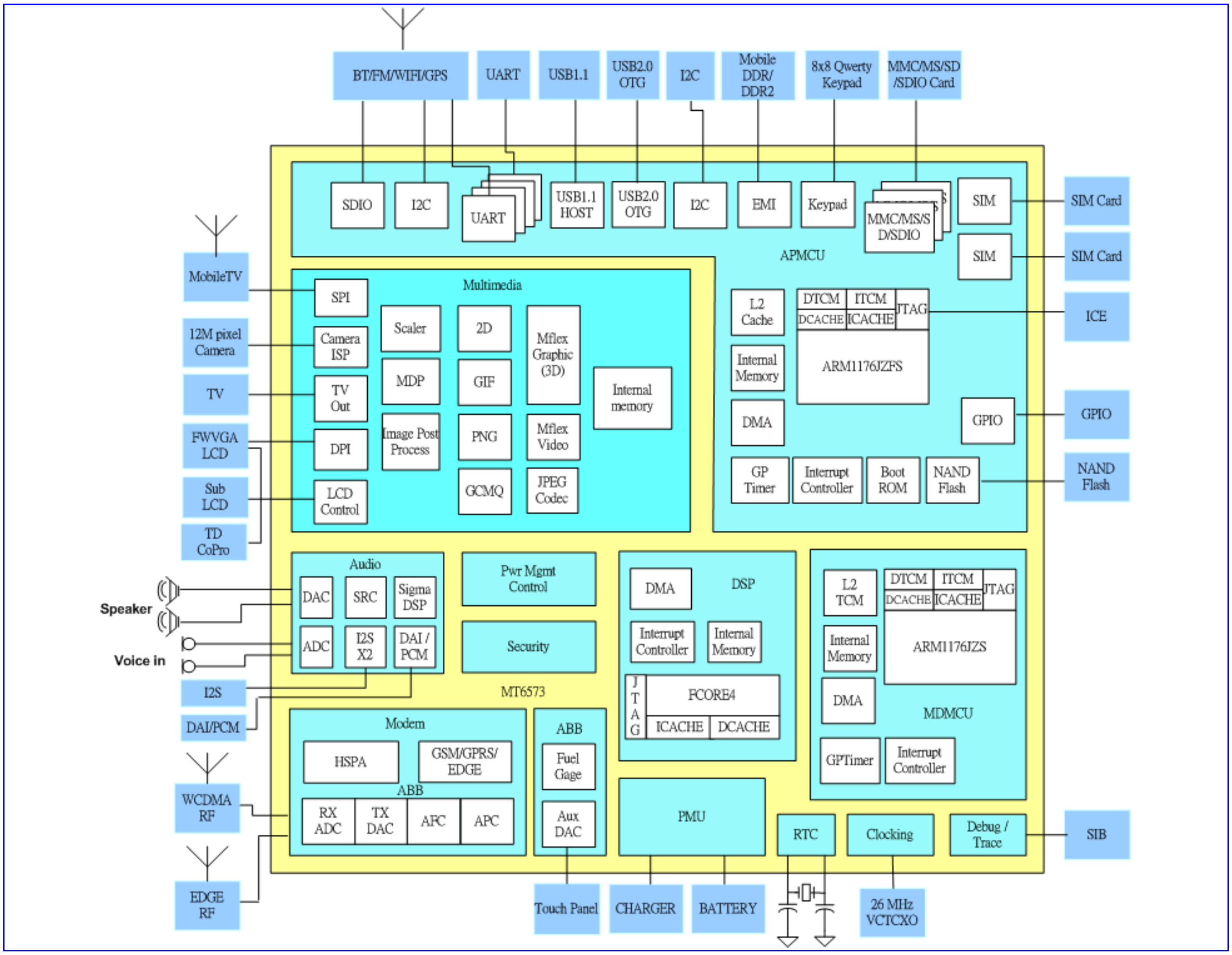


Figure 1 is the block diagram of MT6573.

1.2 Platform Features

- **General**
  - Smart phone two MCU subsystems architecture
  - NAND Flash Bootloader
  - Coresight debug tool
- **AP MCU Subsystem**
  - 676MHz ARM1176 MCU core for Applications/MMI
  - Integrated VFP11 coprocessor (1.35GFLOPS)
  - 32KB I-Cache and 32KB D-Cache
  - 16KB I- and 16KB D- Tightly Couple Memory
  - Dedicated 128KB L2 cache @ 676MHz
  - Shared 128KB FlexL2 scratchpad memory
- **MD MCU Subsystem**
  - ARM1176 MCU with Fcore4 (Dual-MAC 16-bit fixed-point) DSP Modem Cores system
  - Dedicated 32KB I-Cache and 32KB D-Cache
  - 64KB I- and 64KB D- Tightly Couple Memory
  - 96KB L2 Tightly Couple Memory
  - HW based 2G and 3G modems
  - RLC-MAC accelerator
- **External Memory Interface**
  - LPDDR support up to 256MB per device
  - 32-bit data bus width
  - Memory clock up to 200MHz
  - Self-refresh mode support
  - Low power operation
  - Programmable slew rate for memory controller's IO pads
  - 4 external memory devices supported
  - Advanced bandwidth arbitration control
- **Security**
  - ARM™ TrustZone® Security
  - OMTP TR1 Compliance
- **Connectivity**
  - One USB2.0 High Speed OTG port
  - NAND Flash Controller with NAND bootable support
  - 4 UART for GPS, BT, FM-RDS, modem and debug interfaces
  - IrDA FIR/MIR/SIR
  - 2 I2C to control external peripheral devices
  - I2S for connection with optional external hi-end audio codec
  - Multiple GPIOs
  - 4 set Memory Card Controller supporting SD/SDHC/MMC and SDIO2.0 protocol
  - eMMC bootable support
  - Dual SIM card interface
- **Power Management**
  - APMCU support Dynamic Voltage Frequency Scaling range from 0.9 ~ 1.35V with 25mV stepping
  - Low power architecture support Power management states (Normal, Idle, Slow Idle,

Sleep, Power down) compliant with Windows Mobile or Android requirement

- **Operating conditions**
  - Core voltage: 1.2V
  - Processor DVFS voltage : 0.9V ~ 1.35V
  - I/O voltage: 1.8V/2.8V
  - Memory: 1.8V
  - NAND: 1.8V/2.8V
  - LCM interface: 1.8V/2.8V
  - Clock source: 26MHz, 32.768KHz
- **Package**
  - Type : FCCSP
  - Size : 12.6mm x 12.6mm
  - Height : 1mm
  - Ball count : 518 balls
  - Ball pitch : 0.4mm
- **Peripherals**
  - AuxADC with 5 external channels
  - 8x8 Qwerty keypad
  - Touch panel
- **Misc**
  - 4 General Purpose DMA Channel + 17 dedicated DMA Channel
  - 7 PWM
  - TDMA & WCDMA Timer
  - 4 Advanced GPTimer and 3 OSTimer
  - Watchdog Timer

1.3 MODEM Features

- **Modem**
  - Cat. 8 HSDPA (7.2 Mbps)
  - Cat. 6 HSUPA (5.76 Mbps)
  - 4-band EDGE / 4-band 3G
  - Class 12 EDGE, SAIC
- **Audio**
  - Sampling rate support: 6kHz to 96kHz
  - Sample format support: 8-bit/16-bit, Mono/Stereo
  - Interface support: DAI, I2S.
  - 4-band IIR Compensation Filter to enhance loudspeaker response
  - Proprietary audio post-processing technologies: BesEQ, BesHeadphone, Bes3d, BesLive, BesTS, BesBass, BesLoudness.
  - Audio encode: AMR-NB
  - Audio decode: WAV, MP3, AAC, HEAACv1/HEAACv2, AMR-NB, AMR-WB, MIDI/IMY, Vorbis.

1.4 Multimedia Features

- **Display**
  - Support landscape or portrait panel resolution up to FWVGA (864x480)
  - Support 8 / 9 / 16 / 18 / 24-bit host interface (MIPI DBI)
  - Support 8 / 9 / 16 / 24 / 32-bit serial interface
  - Support 16 / 18 / 24-bit RGB interface (MIPI DPI)
  - MIPI DSI interface (2 data lanes)
  - Embedded LCD gamma correction
  - Support true color
  - 6 overlay layers with per-pixel alpha channel and gamma table
  - 2x or 4x temporal dithering
  - Support 32x32 hardware cursor
  - Support NTSC / PAL TV-Out
- **Graphics**
  - OpenGL ES 1.1/2.0 3D Graphic Accelerator capable of processing 16M tri/sec and max. 500M pixel/sec @WVGA resolution
  - OpenVG1.1 Vector Graphics accelerator
  - 2D Graphics HW accelerator
  - Hardware PNG/GIF decoder
- **Image**
  - Integrated image signal processor supporting 5MP up to 15fps and 8MP up to 6fps
  - Support 10-bit Bayer and YUV format
  - Support electronic image stabilization
  - Support video stabilization
  - Support local contrast enhancement
  - Support preference color adjustment
  - Support noise reduction
  - Support edge enhancement (sharpness)
  - Support face detection and visual tracking
  - MIPI CSI-2 high speed camera serial interface support (2 data lanes)
  - Hardware JPEG decode: baseline / progressive with YUV422 / YUV420 / JFIF formats
  - Hardware JPEG encoder: baseline coding
- **Video**
  - H.264 decoder: baseline D1@30fps
  - MPEG-1/2 decoder: D1 @ 30fps
  - MPEG-4 SP / H.263 decoder: FWVGA @ 30fps
  - MPEG-4 decoder: ASP FWVGA @ 30fps
  - H.264 encoder: baseline QVGA @ 30fps
  - MPEG-4 Simple / H.263 encoder: FWVGA @ 30fps

2 Product Description

2.1 Pin Description

2.1.1 Ball Diagram

Package of MT6573: FCCSP 12.6mm*12.6mm, 518-ball, 0.4 mm pitch package. Ball diagrams were shown in **Figure 2**, and the pin coordinate was illustrated in **Table 1**.

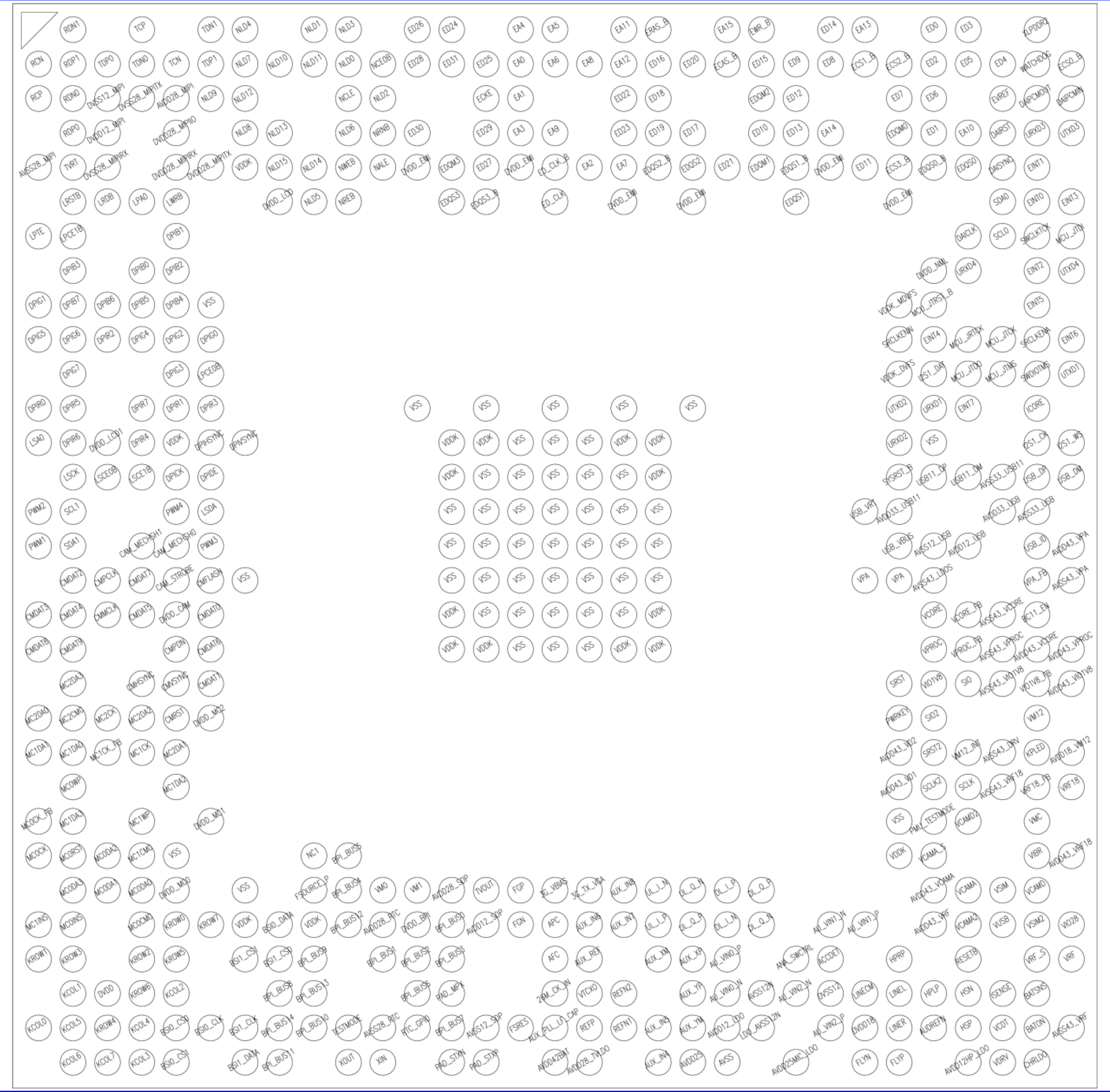


Figure 2 Top view of MT6573 FCCSP 12.6mm*12.6mm, 518-ball, 0.4 mm pitch package

2.1.2 Pin Coordinations

Pin coordinate table with default pin-output is shown in **Table 1**.

Table 1 Pin coordination of ADMUX pin-out

	Ball Name		Ball Name		Ball Name
B1	RCN	B10	NLD0	AG22	DL_Q_N
C1	RCP	C10	NCLE	AJ22	AVSS12N
E1	AVSS28_MIPI	D10	NLD6	AK22	LDO_AVSS12N
G1	LPTE	E10	NWEB	B23	ED9
J1	DPIG1	F10	NREB	C23	ED12
K1	DPIG5	AE10	BPI_BUS5	D23	ED13
M1	DPIR0	AF10	BPI_BUS4	E23	EDQS1_B
N1	LSA0	AG10	BPI_BUS12	F23	EDQS1
R1	PWM2	AK10	TESTMODE	AH23	ANA_SWCTRL
T1	PWM1	AL10	XOUT	AJ23	AU_VIN2_N
V1	CMDAT3	B11	NCE0B	AL23	AVDD25MIC_LDO
W1	CMDAT8	C11	NLD2	A24	ED14
AA1	MC2DA0	D11	NRNB	B24	ED8
AB1	MC1DA1	E11	NALE	D24	EA14
AD1	MC0CK_FB	AF11	VM0	E24	DVDD_EMI
AE1	MC0CK	AG11	AVDD28_RTC	AG24	AU_VIN1_N
AG1	MC1INS	AH11	BPI_BUS1	AH24	ACCDET
AH1	KROW1	AK11	AVSS28_RTC	AJ24	DVSS12
AK1	KCOL0	AL11	XIN	AK24	AU_VIN2_P
A2	RDN1	A12	ED26	A25	EA13
B2	RDP1	B12	ED28	B25	ECS1_B
C2	RDN0	D12	ED30	E25	ED11
D2	RDP0	E12	DVDD_EMI	R25	USB_VRT
E2	TVRT	M12	VSS	U25	VPA

F2	LRSTB	AF12	VM1	AG25	AU_VIN1_P
G2	LPCE1B	AG12	DVDD_BPI	AJ25	LINECM
H2	DPIB3	AH12	BPI_BUS2	AK25	DVDD18
J2	DPIB7	AJ12	BPI_BUS6	AL25	FLYN
K2	DPIG6	AK12	RTC_GPIO	B26	ECS2_B
L2	DPIG7	A13	ED24	C26	ED7
M2	DPIR5	B13	ED31	D26	EDQM0
N2	DPIR6	E13	EDQM3	E26	ECS3_B
P2	LSCK	F13	EDQS3	F26	DVDD_EMI
R2	SCL1	N13	VDDK	J26	VDDK_MDVFS
T2	SDA1	P13	VDDK	K26	SRCLKENAI
U2	CMDAT2	R13	VSS	L26	VDDK_DVFS
V2	CMDAT4	T13	VSS	M26	UTXD2
W2	CMDAT9	U13	VSS	N26	URXD2
Y2	MC2DA3	V13	VDDK	P26	SYSRST_B
AA2	MC2CM0	W13	VDDK	R26	AVDD33_USB11
AB2	MC1DA0	AF13	AVDD28_SDP	T26	USB_VBUS
AC2	MC0WP	AG13	BPI_BUS0	U26	VPA
AD2	MC1DA3	AH13	BPI_BUS3	Y26	SRST
AE2	MC0RST	AJ13	PAD_MPX	AA26	PWRKEY
AF2	MC0DA3	AK13	BPI_BUS7	AB26	AVDD43_VD2
AG2	MC0INS	AL13	PAD_STXN	AC26	AVDD43_VD1
AH2	KROW3	B14	ED25	AD26	VSS
AJ2	KCOL1	C14	ECKE	AE26	VDDK
AK2	KCOL5	D14	ED29	AH26	HPRP
AL2	KCOL6	E14	ED27	AJ26	LINEL
B3	TDP0	F14	EDQS3_B	AK26	LINER
C3	DVSS12_MIPI	M14	VSS	AL26	FLYP
D3	DVDD12_MIPI	N14	VDDK	A27	ED0
E3	DVSS28_MIPIRX	P14	VSS	B27	ED2

F3	LRDB	R14	VSS	C27	ED6
J3	DPIB6	T14	VSS	D27	ED1
K3	DPIR2	U14	VSS	E27	EDQS0_B
N3	DVDD_LCD1	V14	VSS	H27	DVDD_NML
P3	LSCE0B	W14	VDDK	J27	MCU_JTRST_B
U3	CMPCLK	AF14	TVOUT	K27	EINT4
V3	CMMCLK	AG14	AVDD12_SDP	L27	I2S1_DAT
AA3	MC2CK	AK14	AVSS12_SDP	M27	URXD1
AB3	MC1CK_FB	AL14	PAD_STXP	N27	VSS
AE3	MC0DA2	A15	EA4	P27	USB11_DP
AF3	MC0DA1	B15	EA0	T27	AVSS12_USB
AJ3	DVDD	C15	EA1	U27	AVSS43_LDOS
AK3	KROW4	D15	EA3	V27	VCORE
AL3	KCOL7	E15	DVDD_EMI	W27	VPROC
A4	TCP	N15	VSS	Y27	VIO1V8
B4	TDN0	P15	VSS	AA27	SIO2
C4	DVSS28_MIPITX	R15	VSS	AB27	SRST2
F4	LPA0	T15	VSS	AC27	SCLK2
H4	DPIB0	U15	VSS	AD27	PMU_TESTMODE
J4	DPIB5	V15	VSS	AE27	VCAMA_S
K4	DPIG4	W15	VSS	AF27	AVDD43_VCAMA
M4	DPIR7	AF15	FGP	AG27	AVDD43_VRF
N4	DPIR4	AG15	FGN	AJ27	HPLP
P4	LSCE1B	AK15	FSRES	AK27	AUDREFN
T4	CAM_MECHSH1	A16	EA5	A28	ED3
U4	CMDAT7	B16	EA6	B28	ED5
V4	CMDAT5	D16	EA9	D28	EA10
Y4	CMHSYNC	E16	ED_CLK_B	E28	EDQS0
AA4	MC2DA2	F16	ED_CLK	G28	DAICLK
AB4	MC1CK	M16	VSS	H28	URXD4

AD4	MC1WP	N16	VSS	K28	MCU_JRTCK
AE4	MC1CM0	P16	VSS	L28	MCU_JTDO
AF4	MC0DA0	R16	VSS	M28	EINT7
AG4	MC0CM0	T16	VSS	P28	USB11_DM
AH4	KROW2	U16	VSS	T28	AVDD12_USB
AJ4	KROW6	V16	VSS	V28	VCORE_FB
AK4	KCOL4	W16	VSS	W28	VPROC_FB
AL4	KCOL3	AF16	3G_VBIAS	Y28	SIO
B5	TCN	AG16	APC	AB28	VM12_INT
C5	AVDD28_MIPI	AH16	AFC	AC28	SCLK
D5	DVDD28_MIPIIO	AJ16	26M_CK_IN	AD28	VCAMD2
E5	DVDD28_MIPIRX	AK16	AUX_PLL_LF_CAP	AF28	VCAMA
F5	LWRB	AL16	AVDD42BAT	AG28	VCAMA2
G5	DPIB1	B17	EA8	AH28	RESETB
H5	DPIB2	E17	EA2	AJ28	HSN
J5	DPIB4	N17	VSS	AK28	HSP
K5	DPIG2	P17	VSS	AL28	AVDD12HP_LDO
L5	DPIG3	R17	VSS	B29	ED4
M5	DPIR1	T17	VSS	C29	EVREF
N5	VDDK	U17	VSS	D29	DAIRST
P5	DPICK	V17	VSS	E29	DAISYNC
R5	PWM4	W17	VSS	F29	SDA0
T5	CAM_MECHSH0	AF17	3G_TX_VGA	G29	SCL0
U5	CAM_STROBE	AG17	AUX_IN6	K29	MCU_JTCK
V5	DVDD_CAM	AH17	AUX_REF	L29	MCU_JTMS
W5	CMPDN	AJ17	VTCXO	P29	AVSS33_USB11
Y5	CMVSYNC	AK17	REFP	R29	AVDD33_USB
AA5	CMRST	AL17	AVDD28_TVLDO	V29	AVSS43_VCORE
AB5	MC2DA1	A18	EA11	W29	AVSS43_VPROC
AC5	MC1DA2	B18	EA12	Y29	AVSS43_VIO1V8

AE5	VSS	C18	ED22	AB29	AVSS43_DRV
AF5	DVDD_MC0	D18	ED23	AC29	AVSS43_VRF18
AG5	KROW0	E18	EA7	AF29	VSIM
AH5	KROW5	F18	DVDD_EMI	AG29	VUSB
AJ5	KCOL2	M18	VSS	AJ29	ISENSE
AK5	BSI0_CS0	N18	VDDK	AK29	VCDT
AL5	BSI0_CS1	P18	VSS	AL29	VDRV
A6	TDN1	R18	VSS	A30	XLPDDR2
B6	TDP1	T18	VSS	B30	WATCHDOG
C6	NLD9	U18	VSS	C30	DAIPCMOUT
E6	DVDD28_MIPITX	V18	VSS	D30	URXD3
J6	VSS	W18	VDDK	E30	EINT1
K6	DPIG0	AF18	AUX_IN8	F30	EINT0
L6	LPCE0B	AG18	AUX_IN7	G30	SWCLKTCK
M6	DPIR3	AJ18	REFN2	H30	EINT2
N6	DPIHSYNC	AK18	REFN1	J30	EINT5
P6	DPIDE	A19	ERAS_B	K30	SRCLKENA
R6	LSDA	B19	ED16	L30	SWDIOTMS
T6	PWM3	C19	ED18	M30	ICORE
U6	CMFLASH	D19	ED19	N30	I2S1_CK
V6	CMDAT0	E19	EDQS2_B	P30	USB_DP
W6	CMDAT6	N19	VDDK	R30	AVSS33_USB
Y6	CMDAT1	P19	VDDK	T30	USB_ID
AA6	DVDD_MC2	R19	VSS	U30	VPA_FB
AD6	DVDD_MC1	T19	VSS	V30	BC11_EN
AG6	KROW7	U19	VSS	W30	AVDD43_VCORE
AK6	BSI0_CLK	V19	VDDK	Y30	VIO1V8_FB
A7	NLD4	W19	VDDK	AA30	VM12
B7	NLD7	AF19	UL_I_N	AB30	KPLED
C7	NLD12	AG19	UL_I_P	AC30	VRF18_FB

D7	NLD8	AH19	AUX_XM	AD30	VMC
E7	VDDK	AK19	AUX_IN5	AE30	VIBR
N7	DPIVSYNC	AL19	AUX_IN4	AF30	VCAMD
U7	VSS	B20	ED20	AG30	VSIM2
AF7	VSS	D20	ED17	AH30	VRF_S
AG7	VDDK	E20	EDQS2	AJ30	BATSNS
AH7	BSI1_CS1	F20	DVDD_EMI	AK30	BATON
AK7	BSI1_CLK	M20	VSS	AL30	CHRLDO
AL7	BSI1_DATA	AF20	UL_Q_N	B31	ECS0_B
B8	NLD10	AG20	UL_Q_P	C31	DAIPCMIN
D8	NLD13	AH20	AUX_XP	D31	UTXD3
E8	NLD15	AJ20	AUX_YP	F31	EINT3
F8	DVDD_LCD	AK20	AUX_YM	G31	MCU_JTDI
AG8	BSI0_DATA	AL20	AVDD25	H31	UTXD4
AH8	BSI1_CS0	A21	EA15	K31	EINT6
AJ8	BPI_BUS8	B21	ECAS_B	L31	UTXD1
AK8	BPI_BUS14	E21	ED21	N31	I2S1_WS
AL8	BPI_BUS11	AF21	DL_I_P	P31	USB_DM
A9	NLD1	AG21	DL_I_N	T31	AVDD43_VPA
B9	NLD11	AH21	AU_VIN0_P	U31	AVSS43_VPA
E9	NLD14	AJ21	AU_VIN0_N	W31	AVDD43_VPROC
F9	NLD5	AK21	AVDD12_LDO	Y31	AVDD43_VIO1V8
AE9	NC1	AL21	AVSS	AB31	AVDD18_VM12
AF9	FSOURCE_P	A22	EWR_B	AC31	VRF18
AG9	VDDK	B22	ED15	AE31	AVDD43_VRF18
AH9	BPI_BUS9	C22	EDQM2	AG31	VIO28
AJ9	BPI_BUS13	D22	ED10	AH31	VRF
AK9	BPI_BUS10	E22	EDQM1	AK31	AVSS43_VRF
A10	NLD3	AF22	DL_Q_P		

2.1.3 Detail Pin Description

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

Table 2 Acronym for pin type

Pin Name	Type	Description	Power Domain
System			
SRCLKENA	DO	Enable signal for 26MHz source clock	DVDD_NML
SRCLKENAI	DI	Force 26MHz source clock enable (tie to GND when not used)	DVDD_NML
SYSRST_B	DI	System reset (active low)	DVDD_NML
ICORE	DI	Test mode control (tie to GND)	DVDD_NML
Baseband Serial Interface			
BSI1_CLK	DIO	Baseband serial interface 1 clock signal	DVDD
BSI1_DATA	DIO	Baseband serial interface 1 data signal	DVDD
BSI1_CS1	DIO	Baseband serial interface 1 chip select signal 1	DVDD
BSI1_CS0	DIO	Baseband serial interface 1 chip select signal 0	DVDD
BSI0_CLK	DIO	Baseband serial interface 0 clock signal	DVDD
BSI0_DATA	DIO	Baseband serial interface 0 data signal	DVDD
BSI0_CS0	DIO	Baseband serial interface 0 chip select signal 0	DVDD
BSI0_CS1	DIO	Baseband serial interface 0 chip select signal 1	DVDD
PA Mode Control			
VM0	DIO	PA mode selection 0	DVDD_BPI
VM1	DIO	PA mode selection 1	DVDD_BPI
Baseband Parallel Interface			
BPI_BUS0	DIO	ASM_VCT1 for ASM switch control	DVDD_BPI
BPI_BUS1	DIO	ASM_VCT2 for ASM switch control	DVDD_BPI
BPI_BUS2	DIO	ASM_VCT3 for ASM switch control	DVDD_BPI
BPI_BUS3	DIO	ASM_VCT4 for ASM switch control	DVDD_BPI

Pin Name	Type	Description	Power Domain
BPI_BUS4	DIO	ASM_VDD for ASM enable control	DVDD_BPI
BPI_BUS5	DIO	PAEN	DVDD_BPI
BPI_BUS6	DIO	BANDSW	DVDD_BPI
BPI_BUS7	DIO	EDGE_MODE	DVDD_BPI
BPI_BUS8	DIO	GPS timing sync.	DVDD
BPI_BUS9	DIO	Reserved for 2G operation window notation	DVDD_BPI
BPI_BUS10	DIO	W_PA1_ON for WCDMA Band 1 PA control	DVDD_BPI
BPI_BUS11	DIO	W_PA2_ON for WCDMA Band 2 PA control	DVDD_BPI
BPI_BUS12	DIO	W_PA5_ON for WCDMA Band 5 PA control	DVDD_BPI
BPI_BUS13	DIO	W_PA8_ON for WCDMA Band 8 PA control	DVDD_BPI
BPI_BUS14	DIO	W_LDO18_EN for WCDMA LDO control	DVDD_BPI
NC1	DIO	TDD timing sync	DVDD_BPI
FSOURCE_P	DIO	For EFUSE burning, tie to GND	DVDD_BPI
UART Interface 1			
URXD1	DIO	UART 1 receive data	DVDD_NML
UTXD1	DIO	UART 1 transmit data	DVDD_NML
UART Interface 2			
URXD2	DIO	UART 2 receive data	DVDD_NML
UTXD2	DIO	UART 2 transmit data	DVDD_NML
UART Interface 3			
URXD3	DIO	UART 3 receive data	DVDD_NML
UTXD3	DIO	UART 3 transmit data	DVDD_NML
UART Interface 4			
URXD4	DIO	UART 4 receive data	DVDD_NML
UTXD4	DIO	UART 4 transmit data	DVDD_NML
Digital Audio Interface			
DAICLK	DIO	DAI clock output	DVDD_NML
DAIPCMOUT	DIO	DAI pcm data output	DVDD_NML
DAIPCMIN	DIO	DAI pcm data input	DVDD_NML
DAISYNC	DIO	DAI reset signal input	DVDD_NML
DAIRST	DIO	DAI frame synchronization signal output	DVDD_NML
ARM JTAG Interface			
MCU_JTRST_B	DIO	MCU JTAG reset	DVDD_NML
MCU_JTCK	DIO	MCU JTAG clock	DVDD_NML
MCU_JTDI	DIO	MCU JTAG data in	DVDD_NML
MCU_JTMS	DIO	MCU JTAG test mode select	DVDD_NML
MCU_JTDO	DIO	MCU JTAG data out	DVDD_NML

Pin Name	Type	Description	Power Domain
MCU_JRTCK	DIO	MCU JTAG return clock	DVDD_NML
FCore4 JTAG Interface			
SWCLKTCK	DIO	DSP JTAG clock	DVDD_NML
SWDIOTMS	DIO	DSP JTAG test mode select	DVDD_NML
PWM			
PWM1	DIO	Pulse width modulated signal 1	DVDD_LCD1
PWM2	DIO	Pulse width modulated signal 2	DVDD_LCD1
PWM3	DIO	Pulse width modulated signal 3	DVDD_LCD1
PWM4	DIO	Pulse width modulated signal 4	DVDD_CAM
External Interrupt			
EINT0	DIO	External interrupt 0	DVDD_NML
EINT1	DIO	External interrupt 1	DVDD_NML
EINT2	DIO	External interrupt 2	DVDD_NML
EINT3	DIO	External interrupt 3	DVDD_NML
EINT4	DIO	External interrupt 4	DVDD_NML
EINT5	DIO	External interrupt 5	DVDD_NML
EINT6	DIO	External interrupt 6	DVDD_NML
EINT7	DIO	External interrupt 7	DVDD_NML
Keypad Interface			
KCOL7	DIO	Keypad column 7	DVDD
KCOL6	DIO	Keypad column 6	DVDD
KCOL5	DIO	Keypad column 5	DVDD
KCOL4	DIO	Keypad column 4	DVDD
KCOL3	DIO	Keypad column 3	DVDD
KCOL2	DIO	Keypad column 2	DVDD
KCOL1	DIO	Keypad column 1	DVDD
KCOL0	DIO	Keypad column 0 (Low => USB download mode)	DVDD
KROW7	DIO	Keypad row 7	DVDD
KROW6	DIO	Keypad row 6	DVDD
KROW5	DIO	Keypad row 5	DVDD
KROW4	DIO	Keypad row 4	DVDD
KROW3	DIO	Keypad row 3	DVDD
KROW2	DIO	Keypad row 2	DVDD
KROW1	DIO	Keypad row 1	DVDD
KROW0	DIO	Keypad row 0	DVDD
I2C Interface			
SCL0	DIO	I2C0 clock	DVDD_NML

Pin Name	Type	Description	Power Domain
SDA0	DIO	I2C0 data	DVDD_NML
SCL1	DIO	I2C1 clock	DVDD_LCD1
SDA1	DIO	I2C1 data	DVDD_LCD1
I2S Interface 0 (no pin out; shared with MIPI)			
I2S0_CK (DAICLK)	DIO	I2C0 clock	DVDD_NML
I2S0_WS (DAISYNC)	DIO	I2S0 word select	DVDD_NML
I2S0_DAT (DAIPCMOUT)	DIO	I2S0 serial data	DVDD_NML
I2S Interface 1			
I2S1_CK	DO	I2C1 clock	DVDD_NML
I2S1_WS	DO	I2S1 word select	DVDD_NML
I2S1_DAT	DO	I2S1 serial data	DVDD_NML
Camera Interface			
CMRST	DIO	Reset control to sensor	DVDD_CAM
CMPDN	DIO	Power down to sensor	DVDD_CAM
CMVSYNC	DIO	Vertical synchronization signal from sensor	DVDD_CAM
CMHSYNC	DIO	Horizontal synchronization signal from sensor	DVDD_CAM
CMDAT9	DIO	Pixel data[9] from sensor / data[7] for YUV422 format	DVDD_CAM
CMDAT8	DIO	Pixel data[8] from sensor / data[6] for YUV422 format	DVDD_CAM
CMDAT7	DIO	Pixel data[7] from sensor / data[5] for YUV422 format	DVDD_CAM
CMDAT6	DIO	Pixel data[6] from sensor / data[4] for YUV422 format	DVDD_CAM
CMDAT5	DIO	Pixel data[5] from sensor / data[3] for YUV422 format	DVDD_CAM
CMDAT4	DIO	Pixel data[4] from sensor / data[2] for YUV422 format	DVDD_CAM
CMDAT3	DIO	Pixel data[3] from sensor / data[1] for YUV422 format	DVDD_CAM
CMDAT2	DIO	Pixel data[2] from sensor / data[0] for YUV422 format	DVDD_CAM
CMDAT1	DIO	Pixel data[1] from sensor	DVDD_CAM
CMDAT0	DIO	Pixel data[0] from sensor	DVDD_CAM
CMPCLK	DIO	Pixel clock from sensor	DVDD_CAM
CMMCLK	DIO	Master clock to sensor	DVDD_CAM
CAM_STROBE	DIO	Camera strobe signal	DVDD_CAM
CMFLASH	DIO	Camera flash control signal	DVDD_CAM
CAM_MECHSH0	DIO	Camera mechanical shutter 0	DVDD_CAM
CAM_MECHSH1	DIO	Camera mechanical shutter 1	DVDD_CAM
Serial LCD Interface			
LSCK	DIO	Serial display interface clock output	DVDD_LCD1
LSA0	DIO	Serial display interface address output	DVDD_LCD1
LSDA	DIO	Serial display interface data	DVDD_LCD1
LSCE0B	DIO	Serial display interface chip select 0 output	DVDD_LCD1

Pin Name	Type	Description	Power Domain
LSCE1B	DIO	Serial display interface chip select 1 output	DVDD_LCD1
LCD Interface			
LPCE1B	DIO	Parallel display interface chip select 1 output	DVDD_LCD1
LPCE0B	DIO	Parallel display interface chip select 0 output	DVDD_LCD1
LPTE	DIO	Parallel display interface tearing effect	DVDD_LCD1
LRSTB	DIO	Parallel display interface reset Signal	DVDD_LCD1
LRDB	DIO	Parallel display interface read Strobe	DVDD_LCD1
LPA0	DIO	Parallel display interface address output	DVDD_LCD1
LWRB	DIO	Parallel display interface write Strobe	DVDD_LCD1
DPIDE	DIO	Data enable signal of DPI	DVDD_LCD1
DPICK	DIO	Clock pin of DPI	DVDD_LCD1
DPIVSYNC	DIO	Vertical synchronization signal of DPI	DVDD_LCD1
DPIHSYNC	DIO	Horizontal synchronization signal of DPI	DVDD_LCD1
DPIR7	DIO	Data pin 7 of DPI R-channel / Data 23 for DBI parallel LCD interface	DVDD_LCD1
DPIR6	DIO	Data pin 6 of DPI R-channel / Data 22 for DBI parallel LCD interface	DVDD_LCD1
DPIR5	DIO	Data pin 5 of DPI R-channel / Data 21 for DBI parallel LCD interface	DVDD_LCD1
DPIR4	DIO	Data pin 4 of DPI R-channel / Data 20 for DBI parallel LCD interface	DVDD_LCD1
DPIR3	DIO	Data pin 3 of DPI R-channel / Data 19 for DBI parallel LCD interface	DVDD_LCD1
DPIR2	DIO	Data pin 2 of DPI R-channel / Data 18 for DBI parallel LCD interface	DVDD_LCD1
DPIR1	DIO	Data pin 1 of DPI R-channel / Data 17 for DBI parallel LCD interface	DVDD_LCD1
DPIR0	DIO	Data pin 0 of DPI R-channel / Data 16 for DBI parallel LCD interface	DVDD_LCD1
DPIG7	DIO	Data pin 7 of DPI G-channel / Data 15 for DBI parallel LCD interface	DVDD_LCD1
DPIG6	DIO	Data pin 6 of DPI G-channel / Data 14 for DBI parallel LCD interface	DVDD_LCD1
DPIG5	DIO	Data pin 5 of DPI G-channel / Data 13 for DBI parallel LCD interface	DVDD_LCD1
DPIG4	DIO	Data pin 4 of DPI G-channel / Data 12 for DBI parallel LCD interface	DVDD_LCD1
DPIG3	DIO	Data pin 3 of DPI G-channel / Data 11 for DBI parallel LCD interface	DVDD_LCD1
DPIG2	DIO	Data pin 2 of DPI G-channel / Data 10 for DBI parallel LCD interface	DVDD_LCD1
DPIG1	DIO	Data pin 1 of DPI G-channel / Data 9 for DBI parallel LCD interface	DVDD_LCD1
DPIG0	DIO	Data pin 0 of DPI G-channel / Data 8 for DBI parallel LCD interface	DVDD_LCD1
DPIB7	DIO	Data pin 7 of DPI B-channel / Data 7 for DBI parallel LCD interface	DVDD_LCD1
DPIB6	DIO	Data pin 6 of DPI B-channel / Data 6 for DBI parallel LCD interface	DVDD_LCD1
DPIB5	DIO	Data pin 5 of DPI B-channel / Data 5 for DBI parallel LCD interface	DVDD_LCD1
DPIB4	DIO	Data pin 4 of DPI B-channel / Data 4 for DBI parallel LCD interface	DVDD_LCD1
DPIB3	DIO	Data pin 3 of DPI B-channel / Data 3 for DBI parallel LCD interface	DVDD_LCD1
DPIB2	DIO	Data pin 2 of DPI B-channel / Data 2 for DBI parallel LCD interface	DVDD_LCD1
DPIB1	DIO	Data pin 1 of DPI B-channel / Data 1 for DBI parallel LCD interface	DVDD_LCD1
DPIB0	DIO	Data pin 0 of DPI B-channel / Data 0 for DBI parallel LCD interface	DVDD_LCD1

Pin Name	Type	Description	Power Domain
NAND Flash Interface			
NLD15	DIO	Parallel NAND-Flash data 15	DVDD_LCD
NLD14	DIO	Parallel NAND-Flash data 14	DVDD_LCD
NLD13	DIO	Parallel NAND-Flash data 13	DVDD_LCD
NLD12	DIO	Parallel NAND-Flash data 12	DVDD_LCD
NLD11	DIO	Parallel NAND-Flash data 11	DVDD_LCD
NLD10	DIO	Parallel NAND-Flash data 10	DVDD_LCD
NLD9	DIO	Parallel NAND-Flash data 9	DVDD_LCD
NLD8	DIO	Parallel NAND-Flash data 8	DVDD_LCD
NLD7	DIO	Parallel NAND-Flash data 7	DVDD_LCD
NLD6	DIO	Parallel NAND-Flash data 6	DVDD_LCD
NLD5	DIO	Parallel NAND-Flash data 5	DVDD_LCD
NLD4	DIO	Parallel NAND-Flash data 4	DVDD_LCD
NLD3	DIO	Parallel NAND-Flash data 3	DVDD_LCD
NLD2	DIO	Parallel NAND-Flash data 2	DVDD_LCD
NLD1	DIO	Parallel NAND-Flash data 1	DVDD_LCD
NLD0	DIO	Parallel NAND-Flash data 0	DVDD_LCD
NAND Flash Interface			
NRNB	DIO	Parallel NAND interface chip ready input	DVDD_LCD
NCLE	DIO	Parallel NAND interface command latch enable output	DVDD_LCD
NALE	DIO	Parallel NAND interface address latch enable output	DVDD_LCD
NWEB	DIO	Parallel NAND interface write strobe output	DVDD_LCD
NREB	DIO	Parallel NAND interface read strobe output	DVDD_LCD
NCE0B	DIO	Parallel NAND interface chip select output	DVDD_LCD
External Memory Interface			
EDQS3	DIO	Data strobe signal 3	DVDD_EMI
EDQS3_B	DIO	Data strobe bar signal 3	DVDD_EMI
EDQM3	DIO	Data mask3	DVDD_EMI
ED31	DIO	Data pin 31	DVDD_EMI
ED30	DIO	Data pin 30	DVDD_EMI
ED29	DIO	Data pin 29	DVDD_EMI
ED28	DIO	Data pin 28	DVDD_EMI
ED27	DIO	Data pin 27	DVDD_EMI
ED26	DIO	Data pin 26	DVDD_EMI
ED25	DIO	Data pin 25	DVDD_EMI
ED24	DIO	Data pin 24	DVDD_EMI
ECKE	DIO	Clock enable	DVDD_EMI

Pin Name	Type	Description	Power Domain
EA0	DIO	Address pin 0	DVDD_EMI
EA1	DIO	Address pin 1	DVDD_EMI
EA2	DIO	Address pin 2	DVDD_EMI
EA3	DIO	Address pin 3	DVDD_EMI
EA4	DIO	Address pin 4	DVDD_EMI
EA5	DIO	Address pin 5	DVDD_EMI
EA6	DIO	Address pin 6	DVDD_EMI
EA7	DIO	Address pin 7	DVDD_EMI
EA8	DIO	Address pin 8	DVDD_EMI
EA9	DIO	Address pin 9	DVDD_EMI
ED_CLK	DIO	Clock signal	DVDD_EMI
ED_CLK_B	DIO	Clock bar signal	DVDD_EMI
ERAS_B	DIO	Row address latch signal (low active)	DVDD_EMI
EA12	DIO	Address pin 12	DVDD_EMI
EA11	DIO	Address pin 11	DVDD_EMI
EDQS2	DIO	Data strobe signal 2	DVDD_EMI
EDQS2_B	DIO	Data strobe bar signal 2	DVDD_EMI
EDQM2	DIO	Data mask 2	DVDD_EMI
ED23	DIO	Data pin 23	DVDD_EMI
ED22	DIO	Data pin 22	DVDD_EMI
ED21	DIO	Data pin 21	DVDD_EMI
ED20	DIO	Data pin 20	DVDD_EMI
ED19	DIO	Data pin 19	DVDD_EMI
ED18	DIO	Data pin 18	DVDD_EMI
ED17	DIO	Data pin 17	DVDD_EMI
ED16	DIO	Data pin 16	DVDD_EMI
EWR_B	DIO	Write signal (low active)	DVDD_EMI
ECAS_ADV_B	DIO	Column address latch signal (low active)	DVDD_EMI
EA15	DIO	Address pin 15	DVDD_EMI
EDQS1	DIO	Data strobe signal 1	DVDD_EMI
EDQS1_B	DIO	Data strobe bar signal1	DVDD_EMI
EDQM1	DIO	Data mask1	DVDD_EMI
ED15	DIO	Data pin 15	DVDD_EMI
ED14	DIO	Data pin 14	DVDD_EMI
ED13	DIO	Data pin 13	DVDD_EMI
ED12	DIO	Data pin 12	DVDD_EMI
ED11	DIO	Data pin 11	DVDD_EMI

Pin Name	Type	Description	Power Domain
ED10	DIO	Data pin 10	DVDD_EMI
ED9	DIO	Data pin 9	DVDD_EMI
ED8	DIO	Data pin 8	DVDD_EMI
ECS3_B	DIO	Chip select bar 3 (low active)	DVDD_EMI
ECS1_B	DIO	Chip select bar 1 (low active)	DVDD_EMI
ECS2_B	DIO	Chip select bar 2 (low active)	DVDD_EMI
ECS0_B	DIO	Chip select bar 0 (low active)	DVDD_EMI
EA10	DIO	Address pin 10	DVDD_EMI
EA14	DIO	Address pin 14	DVDD_EMI
EA13	DIO	Address pin 13	DVDD_EMI
EDQS0	DIO	Data strobe signal 0	DVDD_EMI
EDQS0_B	DIO	Data strobe bar signal 0	DVDD_EMI
EDQM0	DIO	Data mask 0	DVDD_EMI
ED7	DIO	Data pin 7	DVDD_EMI
ED6	DIO	Data pin 6	DVDD_EMI
ED5	DIO	Data pin 5	DVDD_EMI
ED4	DIO	Data pin 4	DVDD_EMI
ED3	DIO	Data pin 3	DVDD_EMI
ED2	DIO	Data pin 2	DVDD_EMI
ED1	DIO	Data pin 1	DVDD_EMI
ED0	DIO	Data pin 0	DVDD_EMI
EVREF	DIO	Tie to GND for LPDDR;	DVDD_EMI
XLPDDR2	DIO	Tie to GND for LPDDR;	DVDD_EMI
WATCHDOG	DIO	Reset external memory device	DVDD_EMI
MS/SD Card Interface 2			
MC2CM0	DIO	Command pin of MSDC2	DVDD_MC2
MC2DA0	DIO	Data0 pin of MSDC2	DVDD_MC2
MC2DA1	DIO	Data1 pin of MSDC2	DVDD_MC2
MC2DA2	DIO	Data2 pin of MSDC2	DVDD_MC2
MC2DA3	DIO	Data3 pin of MSDC2	DVDD_MC2
MC2CK	DIO	Clock pin of MSDC2	DVDD_MC2
MC2CK_FB	DIO	Feedback clock pin of MSDC2	DVDD_MC2
MS/SD Card Interface 0			
MC0CM0	DIO	Command pin of MSDC0	DVDD_MC0
MC0DA0	DIO	Data0 pin of MSDC0	DVDD_MC0
MC0DA1	DIO	Data1 pin of MSDC0	DVDD_MC0
MC0DA2	DIO	Data2 pin of MSDC0	DVDD_MC0

Pin Name	Type	Description	Power Domain
MC0DA3	DIO	Data3 pin of MSDC0	DVDD_MC0
MC0CK	DIO	Clock pin of MSDC0	DVDD_MC0
MC0CK_FB	DIO	Feedback clock pin of MSDC0	DVDD_MC0
MC0WP	DIO	Write protect pin of MSDC0	DVDD_MC0
MC0RST	DIO	Reset pin of MSDC0	DVDD_MC0
MC0INS	DIO	Card insertion pin of MSDC0	DVDD
MS/SD Card Interface 1			
MC1CM0	DIO	Command pin of MSDC1	DVDD_MC1
MC1DA0	DIO	Data0 pin of MSDC1	DVDD_MC1
MC1DA1	DIO	Data1 pin of MSDC1	DVDD_MC1
MC1DA2	DIO	Data2 pin of MSDC1	DVDD_MC1
MC1DA3	DIO	Data3 pin of MSDC1	DVDD_MC1
MC1CK	DIO	Clock pin of MSDC1	DVDD_MC1
MC1CK_FB	DIO	Feedback clock pin of MSDC1	DVDD_MC1
MC1WP	DIO	Write protect pin of MSDC1	DVDD_MC1
MC1INS	DIO	Card insertion pin of MSDC1	DVDD
MIPI Interface			
RDN0	AIO	CSI2 data lane 0	DVDD28_MIPIIO
RDP0	AIO	CSI2 data lane 0	DVDD28_MIPIIO
RDN1	AIO	CSI2 data lane 1	DVDD28_MIPIIO
RDP1	AIO	CSI2 data lane 1	DVDD28_MIPIIO
RCN	AIO	CSI2 clock lane	DVDD28_MIPIIO
RCP	AIO	CSI2 clock lane	DVDD28_MIPIIO
TVRT	AIO	Connect to 1.8KOhm 1% resistor to generate bias current	DVDD28_MIPIIO
TDP0	AIO	DSI data lane 0	DVDD28_MIPIIO
TDN0	AIO	DSI data lane 0	DVDD28_MIPIIO
TDP1	AIO	DSI data lane 1	DVDD28_MIPIIO
TDN1	AIO	DSI data lane 1	DVDD28_MIPIIO
TCP	AIO	DSI clock lane	DVDD28_MIPIIO
TCN	AIO	DSI clock lane	DVDD28_MIPIIO
IC-USB			
USB11_DM	AIO	USB D- differential data line	AVDD33_USB11
USB11_DP	AIO	USB D+ differential data line	AVDD33_USB11
USB 2.0			
USB_VBUS	AI	Power for connected device +3.3V	AVDD33_USB
USB_DM	AIO	USB D- differential data line	AVDD33_USB
USB_DP	AIO	USB D+ differential data line	AVDD33_USB

Pin Name	Type	Description	Power Domain
USB_VRT	AO	USB output for bias current; connect with 5.11K 1% Ohm to GND	AVDD33_USB
USB_ID	AI	Identifier pin for USB OTG	AVDD12_USB
Serial Debug Port			
PAD_STXP	AIO	SATA TX+ signal	AVDD12_SDP
PAD_STXN	AIO	SATA TX- signal	AVDD12_SDP
PAD_MPX	AIO	SATA multipath X; connect to GND if not used	AVDD28_SDP
TVOUT Interface			
TVOUT	AO	TV output signal	AVDD28_TVLDO
Power Management Unit			
BC11_EN	AI	BC1.1 charger support enable (tie to GND if charger doesn't support BC1.1)	AVDD43_VD1
VPA	AO	Buck power output for power amplifier	AVDD43_VCORE
VPA_FB	AI	Feedback sense pin of VPA	AVDD43_VCORE
VIO1V8	AO	Buck power output for 1.8V IO and memory	AVDD43_VCORE
VIO1V8_FB	AI	Feedback sense pin of 1.8V IO	AVDD43_VCORE
VCORE	AO	Buck power output for core	AVDD43_VCORE
VCORE_FB	AI	Feedback sense pin of VCORE	AVDD43_VCORE
VPROC	AO	Buck power output for processor	AVDD43_VCORE
VPROC_FB	AI	Feedback sense pin of VPROC	AVDD43_VCORE
VM12_INT	AO	LDO power output for processor memory	AVDD43_VCORE
VM12	AO	LDO power output for memory	AVDD43_VCORE
VRF18_FB	AI	Feedback sense pin of VRF18	AVDD43_VCORE
VRF18	AO	Buck power output for RF 1.8V circuit	AVDD43_VCORE
KPLED	AO	Open drain switch for keypad LED	AVDD43_VCORE
VIBR	AO	LDO power output for vibrator	AVDD43_VD1
VMC	AO	LDO power output for memory card	AVDD43_VD1
VIO28	AO	LDO power output for MIPI/SDP	AVDD43_VD1
VCAMD2	AO	LDO power output for camera	AVDD43_VD1
VCAMD	AO	LDO power output for camera	AVDD43_VD1
VUSB	AO	LDO power output for USB	AVDD43_VD1
VSIM	AO	LDO power output for SIM card, selectable	AVDD43_VD1
VSIM2	AO	LDO power output for SIM2 card, selectable	AVDD43_VD1
VCAMA_S	AI	Feedback sense pin for camera	AVDD43_VD1
VCAMA	AO	LDO power output for camera	AVDD43_VD1
VCAMA2	AO	LDO power output for camera	AVDD43_VD1
VRF_S	AI	Feedback sense pin for VRF	AVDD43_VD1
VRF	AIO	LDO power output for RF chip	AVDD43_VD1

Pin Name	Type	Description	Power Domain
RESETB	AI	Reset signal	AVDD43_VD1
PWRKEY	AI	Power key	AVDD43_VD1
PMU_TESTMODE	AI	Test mode control for PMU	AVDD43_VD1
BATSNS	AI	VBAT sense	AVDD43_VD1
VCDT	AI	Charger-in voltage detection	AVDD43_VD1
ISENSE	AI	Charger current sense	AVDD43_VD1
CHRLDO	AIO	Charger LDO	AVDD43_VD1
VDRV	AO	Output driver for power transistor base	AVDD43_VD1
SIO2	AIO	SIM2 data IO	VSIM2
SRST2	AO	SIM2 reset	VSIM2
SCLK2	AO	SIM2 clock	VSIM2
SCLK	AIO	SIM clock	VSIM
SRST	AO	SIM reset	VSIM
SIO	AO	SIM data IO	VSIM
Analog Baseband			
HSP	AIO	AUDIO_OUT_P for handset receiver	AVDD12HP_LDO
HSN	AIO	AUDIO_OUT_N for handset receiver	AVDD12HP_LDO
HPLP	AIO	Earphone receiver signal for AUDIO_JACK_P	AVDD12HP_LDO
FLYP	AIO	-(Connect to FLYN with 1uF capacitor)	DVDD18
HPRP	AIO	Earphone receiver signal for AUDIO_JACK_R	AVDD12HP_LDO
AUDREFN	AIO	Earphone receiver signal for AUDIO_JACK_GND	AVDD12HP_LDO
FLYN	AIO	-(Connect to FLYP with 1uF capacitor)	DVDD18
LINEL	AIO	Audio interface for FM_LINE_IN_L	AVDD12HP_LDO
LINER	AIO	Audio interface for FM_LINE_IN_R	AVDD12HP_LDO
LINECM	AIO	Audio interface for FM_LINE_IN_CM	AVDD12HP_LDO
ACCDET	AIO	Plug-in/out detection signal for headset	AVDD25
AU_VIN0_P	AIO	Audio 0 in P for microphone	AVDD25_VMIC
AU_VIN0_N	AIO	Audio 0 in N for microphone	AVDD25_VMIC
AU_VIN1_P	AIO	Audio 1 in P for microphone	AVDD25_VMIC
AU_VIN1_N	AIO	Audio 1 in N for microphone	AVDD25_VMIC
AU_VIN2_P	AIO	Audio 2 in P for microphone	AVDD25_VMIC
AU_VIN2_N	AIO	Audio 2 in N for microphone	AVDD25_VMIC
DL_Q_P	AIO	UMTS downlink for UMTSRX_QP	AVDD25
DL_Q_N	AIO	UMTS downlink for UMTSRX_QN	AVDD25
DL_I_N	AIO	UMTS downlink for UMTSRX_IN	AVDD25
DL_I_P	AIO	UMTS downlink for UMTSRX_IP	AVDD25
UL_Q_N	AIO	UMTS uplink for GSM_UMTSTX_QN	AVDD25

Pin Name	Type	Description	Power Domain
UL_Q_P	AIO	UMTS uplink for GSM_UMTSTX_QP	AVDD25
UL_I_P	AIO	UMTS uplink for GSM_UMTSTX_IP	AVDD25
UL_I_N	AIO	UMTS uplink for GSM_UMTSTX_IN	AVDD25
AUX_IN4	AI	Aux ADC external channel 4 for ADC4_USB	AVDD25
AUX_IN5	AI	Aux ADC external channel 5 for ADC5_HOOK_DET	AVDD25
AUX_IN6	AI	Aux ADC external channel 6 for ADC6_UMTS_POWER	AVDD25
AUX_IN7	AI	Aux ADC external channel 7 for ADC7_UMTS_Temp	AVDD25
AUX_IN8	AI	Aux ADC external channel 8 for ADC8_ACCESSORY	AVDD25
AUX_XP	AI	Aux ADC channel for touch screen TP_X+	AVDD25
AUX_XM	AI	Aux ADC channel for touch screen TP_X-	AVDD25
AUX_YP	AI	Aux ADC channel for touch screen TP_Y+	AVDD25
AUX_YM	AI	Aux ADC channel for touch screen TP_Y-	AVDD25
REFN	AI	Reference voltage for LDO, tie to GND	AVDD25
REFP	AI	Reference voltage for LDO, tie to GND with 1uF capacitor	AVDD25
3G_VBIAS	AO	3G voltage bias; connect to W_PA_VBA	VTCXO
3G_TX_VGA	AIO	3G TX variable gain amplifier	VTCXO
AFC	AIO	Automatic frequency control	VTCXO
APC	AIO	Automatic power control	VTCXO
26M_CK_IN	AI	Input pin of 26MHz clock	AVDD12_LDO
FGN	AI	Fuel gauge signal connect to battery GND	AVDD25
FGP	AI	Fuel gauge signal tie to GND	AVDD25
FSRES	AI	Tie to GND with 523Ohm resistor	AVDD28_TVLDO
AUX_PLL_LF_CAP	AI	Tie to GND with 6.8nF capacitor	AVDD25
TVOUT	AO	TV output for VIDEO interface	DVDD18
Real-Time Clock			
XIN	AI	RTC input; connect to 32K oscillator output	AVDD28_RTC
XOUT	AO	RTC output; connect to 32K oscillator input	AVDD28_RTC
TESTMODE	AI	TEST mode control pin; tie to GND	AVDD28_RTC
RTC_GPIO	AIO	RTC GPIO	AVDD28_RTC
Analog Power			
AVDD12HP_LDO	P	Analog power output 1.2V for audio interface	-
AVDD12_LDO	P	Analog power output 1.2V	-
AVDD12_SDP	P	Analog power output 1.2V for serial debug port	-
AVDD12_USB	P	Analog power output 1.2V for USB	-
AVDD18_VM12	P	1.8V power input for memory LDO	-
AVDD25	P	Analog power output 2.5V	-
AVDD25MIC_LDO	P	Analog power output 2.5V for mic	-

Pin Name	Type	Description	Power Domain
AVDD28_TVLDO	P	Analog power output 2.8V for TV	-
AVDD28_SDP	P	Analog power input 2.8V for serial debug port	-
AVDD28_RTC	P	Analog power output 2.8V for real-time clock	-
AVDD28_MIPI	P	Analog power input 2.8V for MIPI	-
AVDD33_USB	P	Analog power output 3.3V for USB	-
AVDD33_USB11	P	Analog power output 3.3V for USB11	-
AVDD42BAT	P	Battery input power for ABB	-
AVDD43_VPA	P	Battery input power for VPA	-
AVDD43_VCORE	P	Battery input power for VCORE	-
AVDD43_VD1	P	Battery input power for LDO group 1	-
AVDD43_VD2	P	Battery input power for LDO group 2	-
AVDD43_VCAMA	P	Battery input power for VCAMA LDO	-
AVDD43_VIO1V8	P	Battery input power for VIO1V8	-
AVDD43_VPROC	P	Battery input power for VPROC	-
AVDD43_VRF18	P	Battery input power for VRF18	-
AVDD43_VRF	P	Battery input power for VRF LDO	-
VTCXO	P	Voltage output for temperature compensated crystal oscillator	VTCXO
Digital Power			
DVDD	P	Digital power input 1.8V	-
DVDD12_MIPI	P	Digital power input 1.2V for MIPI	-
DVDD28_MIPIIO	P	Digital power input 2.8V for MIPIIO	-
DVDD28_MIPITX	P	Digital power input 2.8V for MIPITX	-
DVDD28_MIPIRX	P	Digital power input 2.8V for MIPIRX	-
DVDD18	P	Digital power input 1.8V	-
DVDD_BPI	P	Digital power input for BPI	-
DVDD_BSI	P	Digital power input for BSI	-
DVDD_CAM	P	Digital power input for camera	-
DVDD_EMI	P	Digital power input for EMI	-
DVDD_LCD	P	Digital power input for LCD	-
DVDD_MC0	P	Digital power input for MSDC0	-
DVDD_MC1	P	Digital power input for MSDC1	-
DVDD_MC2	P	Digital power input for MSDC2	-
VDDK	P	Digital power input for core	-
VDDK_DVFS	P	Digital power input for processor	-
VDDK_MDVFS	P	Digital power input for processor memory	-
Analog Ground			
AVSS	G	-	-

Pin Name	Type	Description	Power Domain
AVSS12_SDP	G	-	-
AVSS12_USB	G	-	-
AVSS28_MIPI	G	-	-
AVSS33_RTC	G	-	-
AVSS33_USB	G	-	-
AVSS33_USB11	G	-	-
AVSS43_VPA	G	-	-
AVSS43_DRV	G	-	-
AVSS43_LDOS	G	-	-
AVSS43_VCORE	G	-	-
AVSS43_VIO1V8	G	-	-
AVSS43_VRF18	G	-	-
AVSS43_VRF	G	-	-
AVSS43_VPROC	G	-	-
AVSS12N	G	-	-
LDO_AVSS12N	G	-	-
Digital Ground			
DVSS	G	-	-
DVSS12	G	-	-
DVSS12_MIPI	G	-	-
DVSS28_MIPIIO	G	-	-
DVSS28_MIPITX	G	-	-
DVSS28_MIPIRX	G	-	-
GNDK	G	-	-
VSS	G	-	-

Table 3 PIN Function Description and Power Domain

Abbreviation	Description
I	Input
LO	Low output
HO	High output
XO	Low or high output
PU	Input pull-up
PD	Input pull-down
-	No PU/PD
0~N	Aux. function number
X	Dedicated function pin

Table 4 State of Pins

Name	Reset		Termination When Not Used	IO Type
	State	Aux		
Baseband Serial Interface				
BSI1_CLK	LO	1	No Need	IO Type 2
BSI1_DATA	LO	1	No Need	IO Type 2
BSI1_CS1	LO	1	No Need	IO Type 2
BSI1_CS0	LO	1	No Need	IO Type 2
BSI0_CLK	LO	1	No Need	IO Type 2
BSI0_DATA	LO	1	No Need	IO Type 2
BSI0_CS0	LO	1	No Need	IO Type 2
BSI0_CS1	LO	1	No Need	IO Type 2
PA Mode Control				
VM0	LO	1	No Need	IO Type 2
VM1	LO	1	No Need	IO Type 2
Baseband Parallel Interface				
BPI_BUS12	LO	1	No Need	IO Type 2
BPI_BUS13	LO	1	No Need	IO Type 2
BPI_BUS11	LO	1	No Need	IO Type 2
BPI_BUS9	LO	1	No Need	IO Type 2
BPI_BUS10	LO	1	No Need	IO Type 2
BPI_BUS6	LO	1	No Need	IO Type 2
BPI_BUS5	LO	1	No Need	IO Type 2
BPI_BUS7	LO	1	No Need	IO Type 2
BPI_BUS0	LO	1	No Need	IO Type 2
BPI_BUS14	LO	1	No Need	IO Type 2
BPI_BUS1	LO	1	No Need	IO Type 2
BPI_BUS4	LO	1	No Need	IO Type 2
BPI_BUS2	LO	1	No Need	IO Type 2
BPI_BUS3	LO	1	No Need	IO Type 2
BPI_BUS8	LO	1	No Need	IO Type 2
NC1	LO	-	No Need	IO Type 2
UART Interface 1				
URXD1	PU	1	DVDD_NML	IO Type 2
UTXD1	HO	1	No Need	IO Type 2
UART Interface 2				

Name	Reset		Termination When Not Used	IO Type
	State	Aux		
URXD2	PU	1	DVDD_NML	IO Type 2
UTXD2	HO	1	No Need	IO Type 2
UART Interface 3				
URXD3	PU	1	DVDD_NML	IO Type 2
UTXD3	HO	1	No Need	IO Type 2
UART Interface 4				
URXD4	PU	1	DVDD_NML	IO Type 2
UTXD4	HO	1	No Need	IO Type 2
SIM2 Interface				
SIO2	PD	1	VSS	IO Type 2
SRST2	LO	1	No Need	IO Type 2
SCLK2	LO		No Need	IO Type 2
Digital Audio Interface				
DAICLK	HO	1	No Need	IO Type 2
DAIPCMOUT	LO	1	No Need	IO Type 2
DAIPCMIN	PD	1	VSS	IO Type 2
DAISYNC	LO	1	No Need	IO Type 2
DAIRST	PU	1	DVDD_NML	IO Type 2
ARM11 JTAG Interface				
MCU_JTRST_B	PD	1	VSS	IO Type 2
MCU_JTCK	PU	1	DVDD_NML	IO Type 2
MCU_JTDI	PU	1	DVDD_NML	IO Type 2
MCU_JTMS	PU	1	DVDD_NML	IO Type 2
MCU_JTDO	XO	1	No Need	IO Type 2
MCU_JRTCK	LO	1	No Need	IO Type 2
FCore4 JTAG Interface				
SWCLKTCK	PU	1	DVDD_NML	IO Type 2
SWDIOTMS	PU	1	DVDD_NML	IO Type 2
PWM				
PWM1	LO	1	No Need	IO Type 2
PWM2	LO	1	No Need	IO Type 2
PWM3	LO	1	No Need	IO Type 2
PWM4	LO	1	No Need	IO Type 2
External Interrupt				
EINT0	PU	1	DVDD_NML	IO Type 2
EINT1	PU	1	DVDD_NML	IO Type 2
EINT2	PU	1	DVDD_NML	IO Type 2

Name	Reset		Termination When Not Used	IO Type
	State	Aux		
EINT3	PU	1	DVDD_NML	IO Type 2
EINT4	PU	1	DVDD_NML	IO Type 2
EINT5	PU	1	DVDD_NML	IO Type 2
EINT6	PU	1	DVDD_NML	IO Type 2
EINT7	PU	1	DVDD_NML	IO Type 2
Keypad Interface				
KCOL7	PD	0	No Need	IO Type 2
KCOL6	PD	0	No Need	IO Type 2
KCOL5	PD	0	No Need	IO Type 2
KCOL4	PD	0	No Need	IO Type 2
KCOL3	PD	0	No Need	IO Type 2
KCOL2	PD	0	No Need	IO Type 2
KCOL1	PU	1	DVDD	IO Type 2
KCOL0	PU	1	DVDD	IO Type 2
KROW7	PD	0	No Need	IO Type 2
KROW6	PD	0	No Need	IO Type 2
KROW5	PD	0	No Need	IO Type 2
KROW4	PD	0	No Need	IO Type 2
KROW3	PD	0	No Need	IO Type 2
KROW2	PD	0	No Need	IO Type 2
KROW1	PD	0	No Need	IO Type 2
KROW0	PD	1	No Need	IO Type 2
System				
SRCLKENA	HO	X	No Need	IO Type 2
SRCLKENAI	I	X	VSS	IO Type 2
SYSRST_B	PU	X	DVDD_NML	IO Type 2
ICORE	I	X	VSS	IO Type 2
BC11_EN	I	X	No Need	IO Type 3
I2C Interface				
SCL0	PU	1	DVDD_NML	IO Type 2
SDA0	PU	1	DVDD_NML	IO Type 2
SCL1	PU	1	DVDD_LCD1	IO Type 2
SDA1	PU	1	DVDD_LCD1	IO Type 2
Camera Interface				
CMRST	LO	1	No Need	IO Type 2
CMPDN	LO	1	No Need	IO Type 2
CMVSYNC	PD	1	VSS	IO Type 2

Name	Reset		Termination When Not Used	IO Type
	State	Aux		
CMHSYNC	PD	1	VSS	IO Type 2
CMDAT9	PD	1	VSS	IO Type 2
CMDAT8	PD	1	VSS	IO Type 2
CMDAT7	PD	1	VSS	IO Type 2
CMDAT6	PD	1	VSS	IO Type 2
CMDAT5	PD	1	VSS	IO Type 2
CMDAT4	PD	1	VSS	IO Type 2
CMDAT3	PD	1	VSS	IO Type 2
CMDAT2	PD	1	VSS	IO Type 2
CMDAT1	PD	1	VSS	IO Type 2
CMDAT0	PD	1	VSS	IO Type 2
CMPCLK	PD	1	VSS	IO Type 2
CMMCLK	LO	1	No Need	IO Type 2
CAM_STROBE	PD	1	VSS	IO Type 2
CMFLASH	LO	1	No Need	IO Type 2
CAM_MECHSH0	LO	1	No Need	IO Type 2
CAM_MECHSH1	LO	1	No Need	IO Type 2
Serial LCD Interface				
LSCK	LO	1	No Need	IO Type 2
LSA0	LO	1	No Need	IO Type 2
LSDA	HO	1	No Need	IO Type 2
LSCE0B	HO	1	No Need	IO Type 2
LSCE1B	HO	1	No Need	IO Type 2
LCD Interface				
LPCE1B	HO	1	No Need	IO Type 2
LPCE0B	HO	1	No Need	IO Type 2
LPTE	PD	1	VSS	IO Type 2
LRSTB	HO	1	No Need	IO Type 2
LRDB	HO	1	No Need	IO Type 2
LPA0	LO	1	No Need	IO Type 2
LWRB	HO	1	No Need	IO Type 2
NAND Flash Interface				
NLD15	PD	1	No Need	IO Type 2
NLD14	PD	1	No Need	IO Type 2
NLD13	PD	1	No Need	IO Type 2
NLD12	PD	1	No Need	IO Type 2
NLD11	PD	1	No Need	IO Type 2

Name	Reset		Termination When Not Used	IO Type
	State	Aux		
NLD10	PD	1	No Need	IO Type 2
NLD9	PD	1	No Need	IO Type 2
NLD8	PD	1	No Need	IO Type 2
NLD7	PD	1	No Need	IO Type 2
NLD6	PD	1	No Need	IO Type 2
NLD5	PD	1	No Need	IO Type 2
NLD4	PD	1	No Need	IO Type 2
NLD3	PD	1	No Need	IO Type 2
NLD2	PD	1	No Need	IO Type 2
NLD1	PD	1	No Need	IO Type 2
NLD0	PD	1	No Need	IO Type 2
NAND Flash Interface				
NRNB	PU	1	No Need	IO Type 2
NCLE	LO	1	No Need	IO Type 2
NALE	LO	1	No Need	IO Type 2
NWEB	HO	1	No Need	IO Type 2
NREB	HO	1	No Need	IO Type 2
NCE0B	HO	1	No Need	IO Type 2
External Memory Interface				
EDQS3	I	X	VSS	IO Type 2
EDQS3_B	I	X	VSS	IO Type 2
EDQM3	LO	X	No Need	IO Type 2
ED26	I	X	VSS	IO Type 2
ED24	I	X	VSS	IO Type 2
ED30	I	X	VSS	IO Type 2
ED31	I	X	VSS	IO Type 2
ED27	I	X	VSS	IO Type 2
ED25	I	X	VSS	IO Type 2
ED29	I	X	VSS	IO Type 2
ED28	I	X	VSS	IO Type 2
EDQS1	I	X	VSS	IO Type 2
EDQS1_B	I	X	VSS	IO Type 2
EDQM1	LO	X	No Need	IO Type 2
ED10	I	X	VSS	IO Type 2
ED8	I	X	VSS	IO Type 2
ED14	I	X	VSS	IO Type 2
ED15	I	X	VSS	IO Type 2

Name	Reset		Termination When Not Used	IO Type
	State	Aux		
ED11	I	X	VSS	IO Type 2
ED9	I	X	VSS	IO Type 2
ED13	I	X	VSS	IO Type 2
ED12	I	X	VSS	IO Type 2
EA7	LO	X	No Need	IO Type 2
EA9	LO	X	No Need	IO Type 2
EA4	LO	X	No Need	IO Type 2
EA8	LO	X	No Need	IO Type 2
EA2	LO	X	No Need	IO Type 2
EA3	LO	X	No Need	IO Type 2
EA6	LO	X	No Need	IO Type 2
EA1	LO	X	No Need	IO Type 2
EA5	LO	X	No Need	IO Type 2
EA0	LO	X	No Need	IO Type 2
EA10	LO	X	No Need	IO Type 2
EA11	LO	X	No Need	IO Type 2
EA12	LO	X	No Need	IO Type 2
EA13	LO	X	No Need	IO Type 2
EA14	LO	X	No Need	IO Type 2
ECKE	HO	X	No Need	IO Type 2
ED_CLK	LO	X	No Need	IO Type 2
EA15	LO	X	No Need	IO Type 2
ECS0_B	HO	X	No Need	IO Type 2
ED_CLK_B	LO	X	No Need	IO Type 2
ERAS_B	XO	X	No Need	IO Type 2
ECAS_ADV_B	HO	X	No Need	IO Type 2
EDQS0	I	X	VSS	IO Type 2
EDQS0_B	I	X	VSS	IO Type 2
EDQM0	HO	X	No Need	IO Type 2
ED2	I	X	VSS	IO Type 2
ED0	I	X	VSS	IO Type 2
ED6	I	X	VSS	IO Type 2
ED7	I	X	VSS	IO Type 2
ED3	I	X	VSS	IO Type 2
ED1	I	X	VSS	IO Type 2
ED5	I	X	VSS	IO Type 2
ED4	I	X	VSS	IO Type 2

Name	Reset		Termination When Not Used	IO Type
	State	Aux		
EDQS2	I	X	VSS	IO Type 2
EDQS2_B	I	X	VSS	IO Type 2
EDQM2	LO	X	No Need	IO Type 2
ED18	I	X	VSS	IO Type 2
ED16	I	X	VSS	IO Type 2
ED22	I	X	VSS	IO Type 2
ED23	I	X	VSS	IO Type 2
ED19	I	X	VSS	IO Type 2
ED17	I	X	VSS	IO Type 2
ED21	I	X	VSS	IO Type 2
ED20	I	X	VSS	IO Type 2
EWR_B	HO	X	No Need	IO Type 2
ECS1_B	HO	X	No Need	IO Type 2
ECS2_B	HO	X	No Need	IO Type 2
ECS3_B	HO	X	No Need	IO Type 2
XLPDDR2	I	X	VSS	IO Type 2
WATCHDOG	HO	X	No Need	IO Type 2
MS/SD Card Interface 2				
MC2CM0	LO	1	VSS	IO Type 2
MC2DA0	PU	1	VSS	IO Type 2
MC2DA1	PU	1	VSS	IO Type 2
MC2DA2	PU	1	VSS	IO Type 2
MC2DA3	PU	1	VSS	IO Type 2
MC2CK	LO	1	No Need	IO Type 2
MC2CK_FB	PU	1	VSS	IO Type 2
MS/SD Card Interface 0				
MC0CM0	LO	1	VSS	IO Type 2
MC0DA0	PU	1	VSS	IO Type 2
MC0DA1	PU	1	VSS	IO Type 2
MC0DA2	PU	1	VSS	IO Type 2
MC0DA3	PU	1	VSS	IO Type 2
MC0CK	LO	1	No Need	IO Type 2
MC0CK_FB	PU	1	VSS	IO Type 2
MC0WP	PD	1	VSS	IO Type 2
MC0RST	LO	1	No Need	IO Type 2
MC0INS	PU	1	VSS	IO Type 2
MS/SD Card Interface 1				

Name	Reset		Termination When Not Used	IO Type
	State	Aux		
MC1CM0	LO	1	VSS	IO Type 2
MC1DA0	PU	1	VSS	IO Type 2
MC1DA1	PU	1	VSS	IO Type 2
MC1DA2	PU	1	VSS	IO Type 2
MC1DA3	PU	1	VSS	IO Type 2
MC1CK	LO	1	No Need	IO Type 2
MC1CK_FB	PU	1	VSS	IO Type 2
MC1WP	PD	1	VSS	IO Type 2
MC1INS	LO	1	VSS	IO Type 2
MIPI Interface				
RDN0	LO	1	No Need	IO Type 2
RDP0	I	1	VSS	IO Type 2
RDN1	I	1	VSS	IO Type 2
RDP1	HO	1	No Need	IO Type 2
RCN	I	1	VSS	IO Type 2
RCP	I	1	VSS	IO Type 2
TVRT	HO	1	No Need	IO Type 2
TDP0	HO	1	No Need	IO Type 2
TDN0	LO	1	No Need	IO Type 2
TDP1	HO	1	No Need	IO Type 2
TDN1	HO	1	No Need	IO Type 2
TCP	LO	1	No Need	IO Type 2
TCN	HO	1	No Need	IO Type 2
USB11_DM	X		No Need	
USB11_DP	X		No Need	
USB_VBUS	I		AVDD33_USB	
USB_DM	X		No Need	
USB_DP	X		No Need	
USB_VRT	O		VSS	
USB_ID	I		AVDD12_USB	
PAD_STXP	O	-	No Need	IO Type 2
PAD_STXN	O	-	No Need	IO Type 2
PAD_MPX	I	-	VSS	IO Type 2
XIN	I	-	VSS	IO Type 2
XOUT	O	-	No Need	IO Type 2
TESTMODE	I	-	VSS	IO Type 2
RTC_GPIO	O	-	No Need	IO Type 2

Table 5 Default PIN state

Abbreviation	Description
I	Input
LO	Low output
HO	High output
XO	Low or high output
PU	Pull-up
PD	Pull-down
-	No PU/PD
0~N	Aux. function number
X	Delicate function pin

Table 6 State of Pins

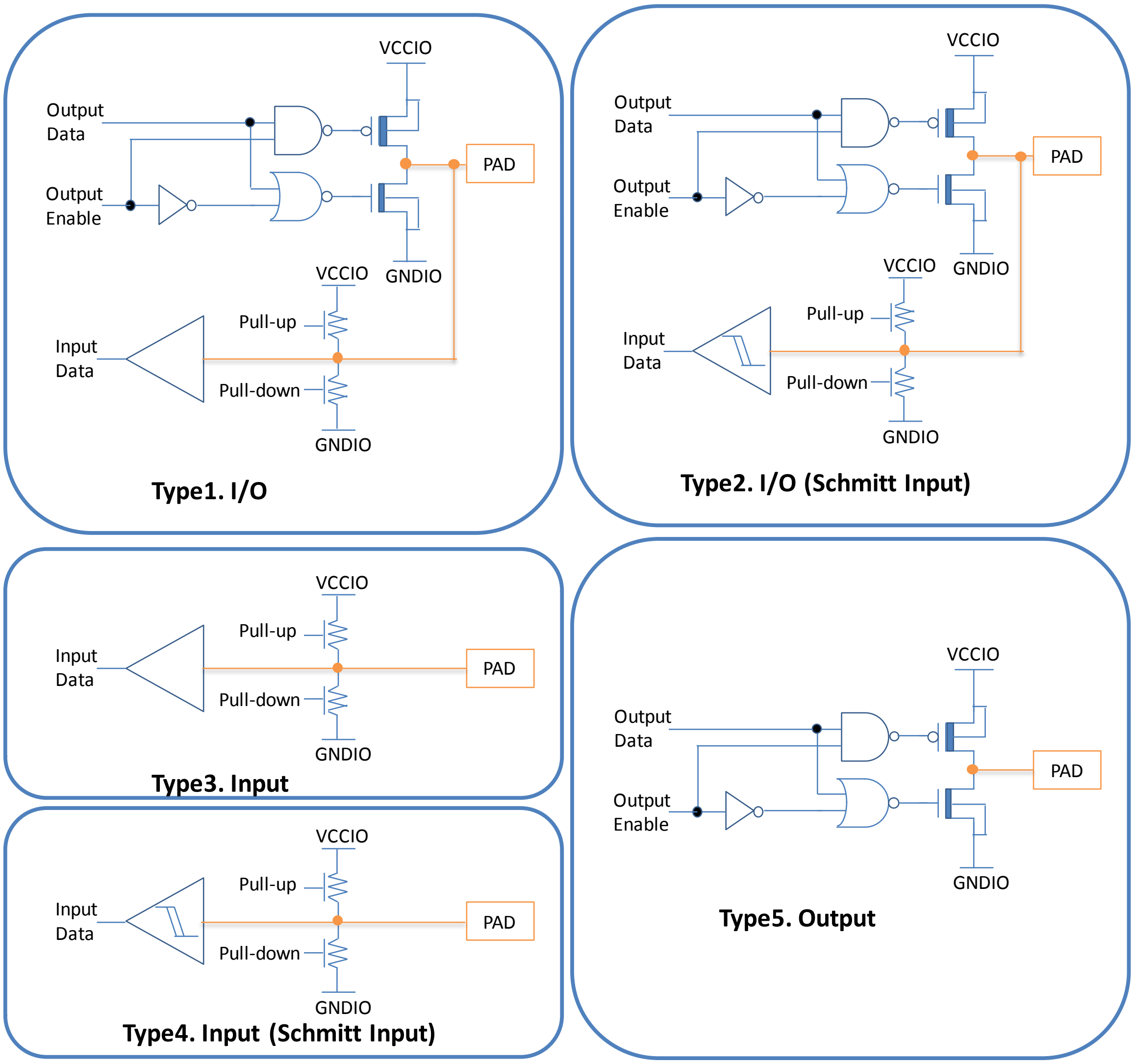


Figure 3 IO Types in State of Pins

2.1.4 Pin Multiplexing, Capability and Settings

Abbreviation	Description
PU	Pull-up, not controllable
PD	Pull-down, not controllable
CU	Pull-up, controllable
CD	Pull-down, controllable
X	Cannot pull-up or pull-down

Table 7 Acronym for Pull-up and Pull-down Type

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
EINT5	0	GPIO0	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	1	EINT5	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	2	I2S0_CK	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	3	CLKM5	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	4	PWM4	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
EINT6	0	GPIO1	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	1	EINT6	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	2	I2S0_WS	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	3	CLKM3	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	4	PWM5	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
EINT7	0	GPIO2	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	1	EINT7	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	2	I2S0_DAT	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	3	CLKM4	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	4	PWM6	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	5	USB_DRVVBUS	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
URXD1	0	GPIO3	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	1	URXD1	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	2	EINT8	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	3	IRDA_RXD	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
UTXD1	0	GPIO4	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	UTXD1	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	2	EINT9	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	3	IRDA_TXD	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
URXD2	0	GPIO5	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
	1	URXD2	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
	2	EINT12	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
UTXD2	0	GPIO6	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_NML
	1	UTXD2	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_NML
	2	EINT13	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_NML
SIO2	0	GPIO7	IO	CU, CD	-	-	VSIM2
	1	PWM1	O	CU, CD	-	-	VSIM2
	2	CLKM0	O	CU, CD	-	-	VSIM2
	3	I2S0_CK	IO	CU, CD	-	-	VSIM2
	4	EINT8	I	CU, CD	-	-	VSIM2

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
SRST2	0	GPIO8	IO	CU, CD	-	-	VSIM2
	1	PWM2	O	CU, CD	-	-	VSIM2
	2	CLKM1	O	CU, CD	-	-	VSIM2
	3	I2S0_WS	IO	CU, CD	-	-	VSIM2
	4	EINT9	I	CU, CD	-	-	VSIM2
SCLK2	0	GPIO9	IO	CU, CD	-	-	VSIM2
	1	PWM3	O	CU, CD	-	-	VSIM2
	2	CLKM2	O	CU, CD	-	-	VSIM2
	3	I2S0_DAT	IO	CU, CD	-	-	VSIM2
	4	EINT10	I	CU, CD	-	-	VSIM2
VM0	0	GPIO10	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_BPI
	1	VM0	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_BPI
	2	URTS2	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_BPI
VM1	0	GPIO11	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_BPI
	1	VM1	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_BPI
	2	UCTS2	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_BPI
BPI_BUS0	0	GPIO12	IO	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
	1	BPI_BUS0	O	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
BPI_BUS1	0	GPIO13	IO	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
	1	BPI_BUS1	O	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
BPI_BUS2	0	GPIO14	IO	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
	1	BPI_BUS2	O	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
BPI_BUS3	0	GPIO15	IO	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
	1	BPI_BUS3	O	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
BPI_BUS4	0	GPIO16	IO	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
	1	BPI_BUS4	O	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
BPI_BUS5	0	GPIO17	IO	CU, CD	2mA	0	DVDD_BPI
	1	BPI_BUS5	O	CU, CD	2mA	0	DVDD_BPI
BPI_BUS6	0	GPIO18	IO	CU, CD	2mA	0	DVDD_BPI
	1	BPI_BUS6	O	CU, CD	2mA	0 (1)	DVDD_BPI
BPI_BUS7	0	GPIO19	IO	CU, CD	2mA	0	DVDD_BPI
	1	BPI_BUS7	O	CU, CD	2mA	0	DVDD_BPI
BPI_BUS9	0	GPIO20	IO	CU, CD	2mA	0	DVDD_BPI
	1	BPI_BUS9	O	CU, CD	2mA	0	DVDD_BPI
	2	Reserved	-	-	-	-	-
	3	DSP_JTMS	I	CU, CD	2mA	0	DVDD_BPI
BPI_BUS10	0	GPIO21	IO	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
	1	BPI_BUS10	O	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
BPI_BUS11	0	GPIO22	IO	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
	1	BPI_BUS11	O	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
	2	URTS1	O	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
	3	DSP_JTDI	I	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
	4	SDA1	IO	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
BPI_BUS12	0	GPIO23	IO	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
	1	BPI_BUS12	O	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
	2	UCTS	I	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
	3	Reserved	-	-	-	-	-
	4	SCL	IO	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
BPI_BUS13	0	GPIO24	IO	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
	1	BPI_BUS13	O	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
	2	URXD1	I	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
	3	URXD4	I	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
	4	SDA0	IO	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
BPI_BUS14	0	GPIO25	IO	CU, CD	2mA	0	DVDD_BPI
	1	BPI_BUS14	O	CU, CD	2mA	0	DVDD_BPI
	2	UTXD1	O	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
	3	UTXD4	O	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
	4	SCL0	IO	CU, CD	2mA, 6mA (2mA)	0	DVDD_BPI
BPI_BUS8	0	GPIO26	IO	CU, CD	2mA	0	DVDD_BPI
	1	BPI_BUS8	O	CU, CD	2mA	0	DVDD_BPI
	2	GPS_SYNC	O	CU, CD	2mA	0	DVDD_BPI
	3	DSP_JTDO	O	CU, CD	2mA	0	DVDD_BPI
BSI1_CLK	0	GPIO27	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	1	BSI1_CLK	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	URTS2	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
BSI1_DATA	0	GPIO28	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	1	BSI1_DATA	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	UCTS2	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
BSI1_CS1	0	GPIO29	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	1	BSI1_DATA1	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
	2	BSI1_CS1	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	-	-
	3	Reserved	-	-	-	-	-
	4	URTS3	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	5	DSP_JTRST_B	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
BSI1_CS0	0	GPIO30	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	1	BSI1_CS0	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	UCTS3	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	5	DSP_EMU_B	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
BSI0_CLK	0	GPIO31	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	1	BSI0_CLK	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	2	URXD2	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	3	EINT15	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
BSI0_DATA	0	GPIO32	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	1	BSI0_DATA	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	2	UTXD2	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	3	EINT12	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
BSI0_CS1	0	GPIO33	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	1	BSI0_CS1	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	2	URXD3	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	3	UCTS2	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	4	EINT13	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	5	DSP_JTCK	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
BSI0_CS0	0	GPIO34	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	1	BSI0_CS0	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	2	UTXD3	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	3	URTS2	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
	4	EINT14	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD
KCOL7	0	GPIO35	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	KCOL7	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	2	SPI_CS_N	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	3	Reserved	-	-	-	-	-
	4	EINT10	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	5	I2S0_WS	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
KCOL6	0	GPIO36	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	KCOL6	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
	2	SPI_SCK	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	3	Reserved	-	-	-	-	-
	4	EINT11	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	5	I2S0_DAT	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
KCOL5	0	GPIO37	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	KCOL5	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	EINT12	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	5	I2S0_CK	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
KCOL4	0	GPIO38	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	KCOL4	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	2	SPI_ MOSI	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	3	Reserved	-	-	-	-	-
	4	EINT13	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	5	URXD3	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
KCOL3	0	GPIO39	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	KCOL3	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	2	SPI_MISO	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	3	Reserved	-	-	-	-	-
	4	EINT14	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	5	UTXD3	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
KCOL2	0	GPIO40	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	KCOL2	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	PWM4	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	5	URXD1	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
KCOL1	0	GPIO41	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	KCOL1	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	PWM5	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	5	UTXD1	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
KCOL0	0	GPIO42	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_NML
	1	KCOL0	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_NML
KROW7	0	GPIO43	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
	1	KROW7	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	EINT15	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	5	URXD4	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
KROW6	0	GPIO44	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	KROW6	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	EINT12	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	5	UTXD4	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
KROW5	0	GPIO45	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	KROW5	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	EINT13	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	5	PWM6	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
KROW4	0	GPIO46	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	KROW4	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	EINT14	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
KROW3	0	GPIO47	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	KROW3	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	EINT15	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
KROW2	0	GPIO48	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	KROW2	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	IRDA_PDN	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
KROW1	0	GPIO49	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	KROW1	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	IRDA_RXD	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
KROW0	0	GPIO50	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	1	KROW0	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	IRDA_TXD	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
MC0INS	0	GPIO51	IO	CU, CD	4mA	0	DVDD
	1	MC0INS	I	CU, CD	4mA	0	DVDD
	2	PWM6	O	CU, CD	4mA	0	DVDD
	3	CLKM1	O	CU, CD	4mA	0	DVDD
	4	EINT11	I	CU, CD	4mA	0	DVDD
	5	IRDA_PDN	O	CU, CD	4mA	0	DVDD
MC1INS	0	GPIO52	IO	CU, CD	4mA	0	DVDD
	1	MC1INS	I	CU, CD	4mA	0	DVDD
	2	PWM5	O	CU, CD	4mA	0	DVDD
	3	CLKM2	O	CU, CD	4mA	0	DVDD
	4	EINT12	I	CU, CD	4mA	0	DVDD
MC0CM0	0	GPIO53	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_MC0
	1	MC0CM0	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_MC0
MC0DA0	0	GPIO54	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC0
	1	MC0DA0	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC0
MC0DA1	0	GPIO55	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC0
	1	MC0DA1	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC0
MC0DA2	0	GPIO56	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC0
	1	MC0DA2	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC0
MC0DA3	0	GPIO57	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC0
	1	MC0DA3	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC0
MC0CK	0	GPIO58	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_MC0
	1	MC0CK	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_MC0
MC0CK_FB	0	GPIO59	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_MC0
	1	MC0CK_FB	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_MC0
MC0RST	0	GPIO60	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_MC0
	1	MC0RST	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_MC0
MC0WP	0	GPIO61	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC0
	1	MC0WP	I	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC0
MC1CM0	0	GPIO62	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_MC1
	1	MC1CM0	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_MC1
MC1DA0	0	GPIO63	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0 (1)	DVDD_MC1

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
	1	MC1DA0	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0 (1)	DVDD_MC1
	2	MC0DA4	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0 (1)	DVDD_MC1
MC1DA1	0	GPIO64	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC1
	1	MC1DA1	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC1
	2	MC0DA5	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC1
MC1DA2	0	GPIO65	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC1
	1	MC1DA2	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC1
	2	MC0DA6	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC1
MC1DA3	0	GPIO66	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC1
	1	MC1DA3	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC1
	2	MC0DA7	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC1
MC1CK	0	GPIO67	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_MC1
	1	MC1CK	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_MC1
MC1CK_FB	0	GPIO68	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_MC1
	1	MC1CK_FB	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_MC1
MC1WP	0	GPIO69	IO	CU, CD	4mA	0	DVDD_MC1
	1	MC1WP	I	CU, CD	4mA	0	DVDD_MC1
MC2CM0	0	GPIO70	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_MC2
	1	MC2CM0	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_MC2
MC2DA0	0	GPIO71	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC2
	1	MC2DA0	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC2
	2	MC0DA4	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC2
MC2DA1	0	GPIO72	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC2
	1	MC2DA1	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC2
	2	MC0DA5	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC2
MC2DA2	0	GPIO73	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC2
	1	MC2DA2	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC2
	2	MC0DA6	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC2
MC2DA3	0	GPIO74	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC2
	1	MC2DA3	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC2
	2	MC0DA7	IO	CU, CD	4mA, 8mA, 12mA, 16mA (4mA)	0	DVDD_MC2
MC2CK	0	GPIO75	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_MC2
	1	MC2CK	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_MC2
CMMCLK	0	GPIO76	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	1	CMMCLK	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
CMPCLK	0	GPIO77	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	1	DVDD_CAM
	1	CMPCLK	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	1	DVDD_CAM

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
CMRST	0	GPIO78	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	1	CMRST	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
CMPDN	0	GPIO79	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	1	CMPDN	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
CMVSYNC	0	GPIO80	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	1	CMVSYNC	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
CMHSYNC	0	GPIO81	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	1	CMHSYNC	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	2	Reserved	-	-	-	-	-
	3	I2S1_WS	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	4	DSP_GPO2	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	5	TBTXFS	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
CMDAT9	0	GPIO82	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	1	CMDAT9	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	2	Reserved	-	-	-	-	-
	3	I2S1_DAT	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	4	DSP_GPO1	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	5	TBRXEN	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
CMDAT8	0	GPIO83	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	1	CMDAT8	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	2	Reserved	-	-	-	-	-
	3	I2S1_CK	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	4	DSP_GPO0	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	5	TBRXFS	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
CMDAT7	0	GPIO84	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	1	CMDAT7	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	2	Reserved	-	-	-	-	-
	3	SPI_CS_N	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
CMDAT6	0	GPIO85	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	1	CMDAT6	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	2	Reserved	-	-	-	-	-
	3	SPI_SCK	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
CMDAT5	0	GPIO86	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	1	CMDAT5	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	2	Reserved	-	-	-	-	-
CMDAT4	0	GPIO87	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	1	CMDAT4	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
	2	Reserved	-	-	-	-	-
	3	SPI_MOSI	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
CMDAT3	0	GPIO88	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	1	CMDAT3	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	2	Reserved	-	-	-	-	-
	3	SPI_MISO	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
CMDAT2	0	GPIO89	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	1	CMDAT2	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	2	Reserved	-	-	-	-	-
CMDAT1	0	GPIO90	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	1	CMDAT1	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
CMDAT0	0	GPIO91	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	1	CMDAT0	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
SCL1	0	GPIO92	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_LCD1
	1	SCL1	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_LCD1
	2	EINT10	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_LCD1
	3	URXD4	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_LCD1
SDA1	0	GPIO93	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	1	SDA1	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	2	EINT11	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	3	UTXD4	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
PWM4	0	GPIO94	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_CAM
	1	PWM4	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_CAM
	2	Reserved	-	-	-	-	-
	3	EINT7	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_CAM
	4	Reserved	-	-	-	-	-
	5	CLKM3	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_CAM
CMFLASH	0	GPIO95	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	1	CMFLASH	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	2	PWM4	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	3	EINT8	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
CAM_MECHSH0	0	GPIO96	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	1	CAM_MECHSH0	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	2	PWM5	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	3	EINT9	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
CAM_MECHSH1	0	GPIO97	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	1	CAM_MECHSH1	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
	2	PWM6	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	3	EINT10	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
CAM_STROBE	0	GPIO98	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	1	CAM_STROBE	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
	2	Reserved	-	-	-	-	-
	3	EINT11	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_CAM
PWM1	0	GPIO99	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	1	PWM1	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	2	CLKM0	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	3	EINT5	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
PWM2	0	GPIO100	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	1	PWM2	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	2	CLKM1	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	3	EINT6	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
PWM3	0	GPIO101	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	1	PWM3	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	2	usb_drvvbus	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	3	EINT12	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	4	Reserved	-	-	-	-	-
	5	CLKM3	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
LSCK	0	GPIO102	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	1	LSCK	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	2	I2S0_CK	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	3	Reserved	-	-	-	-	-
	4	TDMA_CK	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
LSA0	0	GPIO103	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	1	LSA0	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	2	I2S0_WS	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	3	SCL0	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	4	TDMA_D1	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	5	TDTIRQ	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
LSDA	0	GPIO104	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	1	LSDA	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	2	I2S0_DAT	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	3	SDA0	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	4	TDMA_D0	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	5	TCTIRQ2	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
LSCE0B	0	GPIO105	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	1	LSCE0B	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	CLKM3	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	4	TDMA_FS	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	5	TCTIRQ1	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
LSCE1B	0	GPIO106	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	1	LSCE1B	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	2	EINT13	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	3	CLKM4	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	4	LPCE2B	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	5	TEVTVAL	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
DPICK	0	GPIO107	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPICK	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	IRDA_RXD	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	3	CLKM1	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	4	SCL0	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT10	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIDE	0	GPIO108	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIDE	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	IRDA_TXD	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	3	CLKM2	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	4	SDA0	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT11	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIVSYNC	0	GPIO109	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIVSYNC	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	CLKM3	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	4	SCL1	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT12	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIHSYNC	0	GPIO110	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIHSYNC	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	IRDA_PDN	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	4	SDA1	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT13	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIR7	0	GPIO111	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
	1	DPIR_PO 7	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	SPI_CS_N	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	4	I2S0_CK	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT0	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIR6	0	GPIO112	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIR_PO 6	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	SPI_SCK	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	4	I2S0_WS	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT1	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIR5	0	GPIO113	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIR_PO 5	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	URXD1	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	4	I2S0_DAT	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT2	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIR4	0	GPIO114	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIR_PO 4	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	UTXD1	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	4	I2S1_WS	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT3	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIR3	0	GPIO115	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIR_PO 3	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	CLKM0	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	3	URTS1	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	4	I2S1_DAT	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT4	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIR2	0	GPIO116	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIR_PO 2	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	CLKM5	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	3	UCTS1	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	4	I2S1_CK	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT5	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIR1	0	GPIO117	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIR_PO 1	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
	2	CLKM2	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	3	Reserved	-	-	-	-	-
	4	PWM4	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT6	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIR0	0	GPIO118	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIR_PO0	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	PWM5	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT7	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIG7	0	GPIO119	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIG_PO7	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	Reserved	-	-	-	-	-
	5	EINT8	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIG6	0	GPIO120	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIG_PO6	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	SPI_MOSI	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	4	I2S1_WS	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT9	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIG5	0	GPIO121	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIG_PO5	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	URXD2	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	4	IRDA_RXD	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT10	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIG4	0	GPIO122	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIG_PO4	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	UTXD2	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	4	IRDA_TXD	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT11	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIG3	0	GPIO123	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIG_PO3	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
	3	URST2	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	4	PWM3	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT12	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIG2	0	GPIO124	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIG_PO2	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	UCTS2	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	4	PWM4	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT13	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIG1	0	GPIO125	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIG_PO1	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	PWM6	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	4	I2S1_WS	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT14	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIG0	0	GPIO126	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIG_PO0	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	Reserved	-	-	-	-	-
	5	EINT15	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIB7	0	GPIO127	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIB_PO7	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	SPI_MISO	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	4	I2S1_DAT	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT12	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIB6	0	GPIO128	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIB_PO6	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	URXD3	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	4	I2S1_CK	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT13	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIB5	0	GPIO129	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIB_PO5	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	UTXD3	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
	4	URXD4	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT14	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIB4	0	GPIO130	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIB_PO4	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	URTS3	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	4	UTXD4	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT14	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIB3	0	GPIO131	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIB_PO3	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	UCTS3	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	4	URTS4	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	IRDA_PDN	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIB2	0	GPIO132	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIB_PO2	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	UCTS4	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	PWM1	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIB1	0	GPIO133	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIB_PO1	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	Reserved	-	-	-	-	-
	5	PWM2	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
DPIB0	0	GPIO134	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	DPIB_PO0	IO	PD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
LPCE1B	0	GPIO135	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	LPCE1B	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	NCE1B	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
LPCE0B	0	GPIO136	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	LPCE0B	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	DPIDE	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	3	Reserved	-	-	-	-	-
	4	MC3CM0	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	SPI_CS_N	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
LPTE	0	GPIO137	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	1	LPTE	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	2	DPICK	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	3	IRDA_RXD	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	4	MC3_DA0	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	5	SPI_SCK	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
LRSTB	0	GPIO138	IO	-	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	1	LRSTB	O	-	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	IRDA_TXD	IO	-	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
	4	MC3_DA1	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD1
LRDB	0	GPIO139	IO	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	LRDB	O	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	DPIHSYNC	IO	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	3	Reserved	-	-	-	-	-
	4	MC3_DA2	IO	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	SPI_MOSI	IO	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
LPA0	0	GPIO140	IO	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	LPA0	O	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	MC3DA3	O	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	SPI_MISO	IO	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
LWRB	0	GPIO141	IO	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	1	LWRB	O	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	2	DPIVSYNC	IO	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	3	Reserved	-	-	-	-	-
	4	MC3CK	IO	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
	5	EINT14	I	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD1
TDP1	0	GPIO142	IO	-	-	-	DVDD28_MIPIIO
	1	I2S1_CK	O	-	-	-	DVDD28_MIPIIO
	2	SPI_CS_N	IO	-	-	-	DVDD28_MIPIIO
	3	MC3CK	IO	-	-	-	DVDD28_MIPIIO
	4	IRDA_RXD	IO	-	-	-	DVDD28_MIPIIO
	5	EINT14	I	-	-	-	DVDD28_MIPIIO
TDN1	0	GPIO143	IO	-	-	-	DVDD28_MIPIIO
	1	I2S1_WS	O	-	-	-	DVDD28_MIPIIO

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
	2	SPI_SCK	IO	-	-	-	DVDD28_MIPIIO
	3	MC3DA3	IO	-	-	-	DVDD28_MIPIIO
	4	IRDA_TXD	IO	-	-	-	DVDD28_MIPIIO
	5	EINT15	I	-	-	-	DVDD28_MIPIIO
TCP	0	GPIO144	IO	-	-	-	DVDD28_MIPIIO
	1	I2S1_DAT	O	-	-	-	DVDD28_MIPIIO
	2	Reserved	-	-	-	-	DVDD28_MIPIIO
	3	MC3DA2	IO	-	-	-	DVDD28_MIPIIO
	4	URTS2	O	-	-	-	DVDD28_MIPIIO
	5	EINT12	I	-	-	-	DVDD28_MIPIIO
TCN	0	GPIO145	IO	-	-	-	DVDD28_MIPIIO
	1	I2S0_CK	IO	-	-	-	DVDD28_MIPIIO
	2	SPI_MOSI	IO	-	-	-	DVDD28_MIPIIO
	3	MC3DA1	IO	-	-	-	DVDD28_MIPIIO
	4	UCTS2	I	-	-	-	DVDD28_MIPIIO
	5	EINT13	I	-	-	-	DVDD28_MIPIIO
TDP0	0	GPIO146	IO	-	-	-	DVDD28_MIPIIO
	1	I2S0_WS	IO	-	-	-	DVDD28_MIPIIO
	2	SPI_MISO	IO	-	-	-	DVDD28_MIPIIO
	3	MC3DA0	IO	-	-	-	DVDD28_MIPIIO
	4	URTS3	O	-	-	-	DVDD28_MIPIIO
	5	EINT14	I	-	-	-	DVDD28_MIPIIO
TDN0	0	GPIO147	IO	-	-	-	DVDD28_MIPIIO
	1	I2S0_DAT	IO	-	-	-	DVDD28_MIPIIO
	2	IRDA_PDN	O	-	-	-	DVDD28_MIPIIO
	3	MC3CM0	IO	-	-	-	DVDD28_MIPIIO
	4	UCTS3	I	-	-	-	DVDD28_MIPIIO
	5	EINT15	I	-	-	-	DVDD28_MIPIIO
RDN0	0	GPIO148	IO	-	-	-	DVDD28_MIPIIO
	1	MC2CM0	IO	-	-	-	DVDD28_MIPIIO
	2	I2S0_DAT	IO	-	-	-	DVDD28_MIPIIO
	3	Reserved	-	-	-	-	DVDD28_MIPIIO
	4	Reserved	-	-	-	-	DVDD28_MIPIIO
	5	EINT13	I	-	-	-	DVDD28_MIPIIO
RDP0	0	GPIO149	IO	-	-	-	DVDD28_MIPIIO
	1	MC2DA0	IO	-	-	-	DVDD28_MIPIIO
	2	PWM4	O	-	-	-	DVDD28_MIPIIO

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
	3	DAIRST	I	-	-	-	DVDD28_MIPIIO
	4	Reserved	-	-	-	-	DVDD28_MIPIIO
	5	EINT12	I	-	-	-	DVDD28_MIPIIO
RCN	0	GPIO150	IO	-	-	-	DVDD28_MIPIIO
	1	MC2DA1	IO	-	-	-	DVDD28_MIPIIO
	2	PWM5	O	-	-	-	DVDD28_MIPIIO
	3	DAISYNC	O	-	-	-	DVDD28_MIPIIO
	4	Reserved	-	-	-	-	DVDD28_MIPIIO
	5	EINT11	I	-	-	-	DVDD28_MIPIIO
RCP	0	GPIO151	IO	-	-	-	DVDD28_MIPIIO
	1	MC2DA2	IO	-	-	-	DVDD28_MIPIIO
	2	PWM6	O	-	-	-	DVDD28_MIPIIO
	3	DAIPCMIN	I	-	-	-	DVDD28_MIPIIO
	4	CLKM3	O	-	-	-	DVDD28_MIPIIO
	5	EINT10	I	-	-	-	DVDD28_MIPIIO
RDN1	0	GPIO152	IO	-	-	-	DVDD28_MIPIIO
	1	MC2DA3	IO	-	-	-	DVDD28_MIPIIO
	2	I2S0_CK	IO	-	-	-	DVDD28_MIPIIO
	3	DAIPCMOUT	O	-	-	-	DVDD28_MIPIIO
	4	CLKM2	O	-	-	-	DVDD28_MIPIIO
	5	EINT9	I	-	-	-	DVDD28_MIPIIO
RDP1	0	GPIO153	IO	-	-	-	DVDD28_MIPIIO
	1	MC2CK	IO	-	-	-	DVDD28_MIPIIO
	2	I2S0_WS	IO	-	-	-	DVDD28_MIPIIO
	3	DAICLK	O	-	-	-	DVDD28_MIPIIO
	4	CLKM1	O	-	-	-	DVDD28_MIPIIO
	5	EINT8	I	-	-	-	DVDD28_MIPIIO
NLD15	0	GPIO154	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NLD15	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	2	Reserved	-	-	-	-	-
	3	SPI_CS_N	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	4	CLKM0	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	5	EINT15	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
NLD14	0	GPIO155	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NLD14	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	2	Reserved	-	-	-	-	-
	3	SPI_SCK	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
	4	CLKM1	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	5	EINT14	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
NLD13	0	GPIO156	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NLD13	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	CLKM2	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	5	EINT13	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
NLD12	0	GPIO157	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NLD12	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	2	Reserved	-	-	-	-	-
	3	SPI_MOSI	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	4	CLKM5	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	5	EINT12	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
NLD11	0	GPIO158	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NLD11	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	2	Reserved	-	-	-	-	-
	3	SPI_MISO	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	4	PWM4	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	5	EINT15	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
NLD10	0	GPIO159	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NLD10	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	PWM5	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	5	EINT14	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
NLD9	0	GPIO160	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NLD9	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	PWM6	O	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	5	EINT13	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
NLD8	0	GPIO161	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NLD8	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	Reserved	-	-	-	-	-

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
	5	EINT12	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
NLD7	0	GPIO162	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NLD7	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	2	Reserved	-	-	-	-	-
	3	I2S0_CK	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	4	Reserved	-	-	-	-	DVDD_LCD
	5	EINT11	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
NLD6	0	GPIO163	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NLD7	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	2	Reserved	-	-	-	-	-
	3	I2S0_WS	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	4	Reserved	-	-	-	-	-
	5	EINT10	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
NLD5	0	GPIO164	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NLD7	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	2	Reserved	-	-	-	-	-
	3	I2S0_DAT	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	4	Reserved	-	-	-	-	-
	5	EINT9	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
NLD4	0	GPIO165	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NLD4	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	Reserved	-	-	-	-	-
	5	EINT8	I	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
NLD3	0	GPIO166	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NLD3	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
NLD2	0	GPIO167	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NLD2	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
NLD1	0	GPIO168	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NLD1	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
NLD0	0	GPIO169	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NLD0	IO	CU, CD	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
NRNB	0	GPIO170	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD
	1	NRNB	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_LCD
NCLE	0	GPIO171	IO	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NCLE	O	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
NALE	0	GPIO172	IO	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NALE	O	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
NWEB	0	GPIO173	IO	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NWEB	O	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
NREB	0	GPIO174	IO	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NREB	O	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
NCE0B	0	GPIO175	IO	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
	1	NCE0B	O	-	2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA (10mA)	0	DVDD_LCD
DAICLK	0	GPIO176	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	DAICLK	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	2	I2S0_CK	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	3	IRDA_PDN	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
DAIPCMOUT	0	GPIO177	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	DAIPCMOUT	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	2	I2S0_DAT	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
DAIPCMIN	0	GPIO178	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	DAIPCMIN	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	2	Reserved	-	-	-	-	-
	3	URXD3	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
DAISYNC	0	GPIO179	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	DAISYNC	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	2	I2S0_WS	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	3	UTXD3	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
DAIRST	0	GPIO180	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	DAIRST	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	2	Reserved	-	-	-	-	-
	3	CLKM5	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
SCL0	0	GPIO181	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
	1	SCL0	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
	2	EINT14	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
SDA0	0	GPIO182	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_NML
	1	SDA0	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_NML
	2	EINT15	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_NML
URXD3	0	GPIO183	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
	1	URXD3	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
	2	EINT12	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
	3	UTXD3	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
	4	CLKM3	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
UTXD3	0	GPIO184	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_NML
	1	UTXD3	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_NML
	2	URXD3	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_NML
	3	PWM5	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_NML
	4	CLKM4	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_NML
URXD4	0	GPIO185	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
	1	URXD4	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
	2	EINT14	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
UTXD4	0	GPIO186	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_NML
	1	UTXD4	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_NML
	2	EINT15	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	0	DVDD_NML
EINT0	0	GPIO187	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	1	EINT0	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	2	SPI_CS_N	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
EINT1	0	GPIO188	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	1	EINT1	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	2	SPI_SCK	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	3	Reserved	-	-	-	-	-
	4	IRDA_PDN	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
EINT2	0	GPIO189	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	1	EINT2	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	2	Reserved	-	-	-	-	-
	3	Reserved	-	-	-	-	-
	4	DSP_GPO3	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
EINT3	0	GPIO190	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	1	EINT3	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	2	SPI_MOSI	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	3	Reserved	-	-	-	-	-
	4	PWM6	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
EINT4	0	GPIO191	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	1	EINT4	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	2	SPI_MISO	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	3	Reserved	-	-	-	-	-
	4	HDQ_ONEWIRE	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
MCU_JTRST_B	0	GPIO192	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	1	MCU_JTRST_B	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML

Name	Aux. Func.	Aux. Name	Aux. Type	PU/PD/ CU/CD	Driving (Default)	Schmitt Trigger	Power Domain
MCU_JTCK	0	GPIO193	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	1	MCU_JTCK	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
MCU_JTDI	0	GPIO194	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	MCU_JTDI	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
MCU_JTMS	0	GPIO195	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	MCU_JTMS	I	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
MCU_JTDO	0	GPIO196	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	MCU_JTDO	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
MCU_JRTCK	0	GPIO197	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	MCU_ JRTCK	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
SWCLKTCK	0	GPIO198	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
	1	SWCLKTCK	O	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	1	DVDD_NML
SWDIOTMS	0	GPIO199	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
	1	SWDIOTMS	IO	CU, CD	2mA, 4mA, 6mA, 8mA (6mA)	0	DVDD_NML
I2S1_CK	0	GPIO200	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
	1	I2S0_CK	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
	2	Reserved	-	-	-	-	-
	3	IRDA_RXD	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
	4	URTS4	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
	5	EINT8	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
I2S1_WS	0	GPIO201	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
	1	I2S0_WS	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
	2	Reserved	-	-	-	-	-
	3	IRDA_TXD	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
	4	UCTS4	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
	5	EINT9	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
I2S1_DAT	0	GPIO202	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
	1	I2S0_DAT	IO	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
	2	Reserved	-	-	-	-	-
	3	IRDA_PDN	O	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML
	4	Reserved	-	-	-	-	-
	5	EINT13	I	CU, CD	4mA, 8mA, 12mA, 16mA (12mA)	1	DVDD_NML

Table 8 Pin Multiplexing, Capability and Settings

2.2 Electrical Characteristics

2.2.1 Absolute Maximum Ratings

Symbol or Pin Name	Description	Min.	Max.	Unit
AVDD12HP_LDO	Analog power output 1.2V for audio interface	1.0	1.32	V
AVDD12_LDO	Analog power output 1.2V	1.0	1.32	V
AVDD12_SDP	Analog power output 1.2V for serial debug port	1.0	1.32	V
AVDD12_USB	Analog power output 1.2V for USB	1.0	1.32	V
AVDD18_VM12	1.8V power input for memory LDO	1.62	2.0	V
AVDD25	Analog power output 2.5V	2.3	2.7	V
AVDD25MIC_LDO	Analog power output 2.5V for mic	2.3	2.7	V
AVDD28_TVLDO	Analog power output 2.8V for TV	2.6	3.0	V
AVDD28_SDP	Analog power input 2.8V for serial debug port	2.6	3.0	V
AVDD28_MIPI	Analog power input 2.8V for MIPI	1.62 (GIO Mode) 2.6 (MIPI/GIO Mode)	2.0 (GIO Mode) 3.0 (MIPI/GIO Mode)	V
AVDD28_RTC	Analog power output 2.8V for real-time clock	1.0	3.0	V
AVDD33_USB	Analog power output 3.3V for USB	3.0	3.6	V
AVDD33_USB11	Analog power output 3.3V for USB11	3.0	3.6	V
AVDD42BAT	Battery input power for ABB	3.4	4.3	V
AVDD43_VPA	Battery input power for VPA	3.4	4.3	V
AVDD43_VCORE	Battery input power for VCORE	3.4	4.3	V
AVDD43_VD1	Battery input power for LDO group 1	3.4	4.3	V
AVDD43_VD2	Battery input power for LDO group 2	3.4	4.3	V
AVDD43_VCAMA	Battery input power for VCAMA LDO	3.4	4.3	V
AVDD43_VIO1V8	Battery input power for VIO1V8	3.4	4.3	V
AVDD43_VPROC	Battery input power for VPROC	3.4	4.3	V
AVDD43_VRF18	Battery input power for VRF18	3.4	4.3	V
AVDD43_VRF	Battery input power for VRF LDO	3.4	4.3	V
DVDD	Digital power input 1.8V	1.62	2.0	V
DVDD12_MIPI	Digital power input 1.2V for MIPI	1.0	1.32	V
DVDD28_MIPIIO	Digital power input 2.8V for MIPIIO	1.62 (GIO Mode) 2.6 (MIPI/GIO Mode)	2.0 (GIO Mode) 3.0 (MIPI/GIO Mode)	V
DVDD28_MIPITX	Digital power input 2.8V for MIPITX	1.62 (GIO Mode) 2.6 (MIPI/GIO Mode)	2.0 (GIO Mode) 3.0 (MIPI/GIO Mode)	V
DVDD28_MIPIRX	Digital power input 2.8V for MIPIRX	1.62 (GIO Mode) 2.6 (MIPI/GIO Mode)	2.0 (GIO Mode) 3.0 (MIPI/GIO Mode)	V
DVDD18	Digital power input 1.8V	1.62	2.0	V
DVDD_BPI	Digital power input for BPI	2.6	3.0	V
DVDD_BSI	Digital power input for BSI	1.62	2.0	V
DVDD_CAM	Digital power input for camera	1.62	3.3	V
DVDD_EMI	Digital power input for EMI	1.62	2.0	V
DVDD_LCD	Digital power input for LCD	1.62	3.3	V
DVDD_MC0	Digital power input for MSDC0	1.62	3.3	V
DVDD_MC1	Digital power input for MSDC1	1.62	3.3	V

Symbol or Pin Name	Description	Min.	Max.	Unit
DVDD_MC2	Digital power input for MSDC2	1.62	3.3	V
VDDK	Digital power input for core	0.9	1.32	V
VDDK_DVFS	Digital power input for processor	0.9	1.44	V
VDDK_MDVFS	Digital power input for processor memory	1.2	1.44	V

Table 9 Absolute Maximum Ratings for Power Supply

Symbol or Pin Name	Description	Min.	Max.	Unit
VDDIO	Supply voltage of IO power	-0.3	4.0	V
VIN	Input voltage of IO voltage	-0.3	4.0	V

Table 10 Absolute Maximum Ratings for Voltage Input

Warning: Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. These are stress ratings only.

2.2.2 Recommended Operating Conditions

Symbol or Pin Name	Description	Min.	Typ.	Max.	Unit
AVDD12HP_LDO	Analog power output 1.2V for audio interface	1.2	1.25	1.3	V
AVDD12_LDO	Analog power output 1.2V	1.2	1.25	1.3	V
AVDD12_SDP	Analog power output 1.2V for serial debug port	1.0	1.2	1.32	V
AVDD12_USB	Analog power output 1.2V for USB	1.0	1.2	1.32	V
AVDD18_VM12	1.8V power input for memory LDO	1.62	1.8	2.0	V
AVDD25	Analog power output 2.5V	2.4	2.5	2.6	V
AVDD25MIC_LDO	Analog power output 2.5V for mic	2.4	2.5	2.6	V
AVDD28_TVLDO	Analog power output 2.8V for TV	2.6	2.8	3.0	V
AVDD28_SDP	Analog power input 2.8V for serial debug port	2.6	2.8	3.0	V
AVDD28_MIPI	Analog power input 2.8V for MIPI	1.62 (GIO Mode) 2.6 (MIPI/GIO Mode)	1.8 (GIO Mode) 2.8 (MIPI/GIO Mode)	2.0 (GIO Mode) 3.0 (MIPI/GIO Mode)	V
AVDD28_RTC	Analog power output 2.8V for real-time clock	1.0	2.8	3.0	V
AVDD33_USB	Analog power output 3.3V for USB	3.0	3.3	3.6	V
AVDD33_USB11	Analog power output 3.3V for USB11	3.0	3.3	3.6	V
AVDD42BAT	Battery input power for ABB	3.4	3.8	4.2	V
AVDD43_VPA	Battery input power for VPA	3.4	3.8	4.2	V
AVDD43_VCORE	Battery input power for VCORE	3.4	3.8	4.2	V
AVDD43_VD1	Battery input power for LDO group 1	3.4	3.8	4.2	V
AVDD43_VD2	Battery input power for LDO group 2	3.4	3.8	4.2	V
AVDD43_VCAMA	Battery input power for VCAMA LDO	3.4	3.8	4.2	V
AVDD43_VIO1V8	Battery input power for VIO1V8	3.4	3.8	4.2	V
AVDD43_VPROC	Battery input power for VPROC	3.4	3.8	4.2	V

Symbol or Pin Name	Description	Min.	Typ.	Max.	Unit
AVDD43_VRF18	Battery input power for VRF18	3.4	3.8	4.2	V
AVDD43_VRF	Battery input power for VRF LDO	3.4	3.8	4.2	V
DVDD	Digital power input 1.8V	1.62	1.8	2.0	V
DVDD12_MIPI	Digital power input 1.2V for MIPI	1.0	1.2	1.32	V
DVDD28_MIPIIO	Digital power input 2.8V for MIPIIO	1.62 (GIO Mode) 2.6 (MIPI/GIO Mode)	1.8 (GIO Mode) 2.8 (MIPI/GIO Mode)	2.0 (GIO Mode) 3.0 (MIPI/GIO Mode)	V
DVDD28_MIPITX	Digital power input 2.8V for MIPITX	1.62 (GIO Mode) 2.6 (MIPI/GIO Mode)	1.8 (GIO Mode) 2.8 (MIPI/GIO Mode)	2.0 (GIO Mode) 3.0 (MIPI/GIO Mode)	V
DVDD28_MIPIRX	Digital power input 2.8V for MIPIRX	1.62 (GIO Mode) 2.6 (MIPI/GIO Mode)	1.8 (GIO Mode) 2.8 (MIPI/GIO Mode)	2.0 (GIO Mode) 3.0 (MIPI/GIO Mode)	V
DVDD18	Digital power input 1.8V	1.62	1.8	2.0	V
DVDD_BPI	Digital power input for BPI	2.6	2.8	3.0	V
DVDD_BSI	Digital power input for BSI	1.62	1.8	2.0	V
DVDD_CAM	Digital power input for camera	1.62	1.8	2.0	V
DVDD_EMI	Digital power input for EMI	1.62	1.8	2.0	V
DVDD_LCD	Digital power input for LCD	1.62	1.8	2.0	V
DVDD_MC0	Digital power input for MSDC0	3.0	3.3	3.6	V
DVDD_MC1	Digital power input for MSDC1	3.0	3.3	3.6	V
DVDD_MC2	Digital power input for MSDC2	3.0	3.3	3.6	V
VDDK	Digital power input for core	1.14	1.2	1.32	V
VDDK_DVFS	Digital power input for processor	1.29	1.35	1.41	V
VDDK_MDVFS	Digital power input for processor memory	1.29	1.35	1.41	V

Table 11 Recommended Operating Conditions for Power Supply

2.2.3 Electrical Characteristics under Recommended Operating Conditions

AC&DC Electrical Characteristics and Operating Conditions of 3.3V Applications (JESD8-B)						
Parameter	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**	**Note**
Tc	Operating temperature	-40	25	125	°C	1
Freq	Maximum operating frequency			**100**	Mhz	1
VDD	Supply voltage of core power	**1.15**	**1.225**	**1.32**	V	1,**4**
VDDIO	Supply voltage of IO power	**2.97**	**3.3**	**3.63**	V	1
Tc	Operating temperature	-40	25	125	°C	1
Inputs						

AC&DC Electrical Characteristics and Operating Conditions of 3.3V Applications (JESD8-B)						
Parameter	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**	**Note**
VIH	Input logic low voltage	2.0		VDDIO+0.3	V	2
VIL	Input logic high voltage	-0.3		0.8	V	2
Rpu	Input pull-up resistance	40	75	190	KW	VDDIO=typ. Vinput=0V
Rpd	Input pull-down resistance	40	75	190	KW	VDDIO=typ. Vinput=3.3V
Outputs						
VOH(DC)	DC Output logic low voltage	2.4			V	VDDIO=min, IOH= - 2mA
VOL(DC)	DC Output logic high voltage			0.4	V	VDDIO=min, IOL= -2mA
Leakage						
IIN	Input leakage current (any input 0V<VIN<VDDIO)	-5		5	mA	**3**
IOZ	Tri-state output leakage current	-5		5	mA	**3**
IIN	Input leakage current (VIN=5.5V/0V) for 5V tolerant IO	-10		10	mA	**3**
IOZ	Tri-state output leakage current for 5V tolerant IO	-10		10	mA	**3**

Table 12 Electrical Characteristics of IO under 3.3V

AC&DC Electrical Characteristics and Operating Conditions of 2.8V Applications (JESD8-B)						
Parameter	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**	**Note**
Tc	Operating temperature	-40	25	125	°C	1
Freq	Maximum operating frequency			**100**	Mhz	1
VDD	Supply voltage of core power	**1.15**	**1.225**	**1.32**	V	1,**4**
VDDIO	Supply voltage of IO power	**2.52**	**2.8**	**3.08**	V	1
Tc	Operating temperature	-40	25	125	°C	1
Inputs						
VIH	Input logic low voltage	0.75*VDDIO		VDDIO+0.3	V	2
VIL	Input logic high voltage	-0.3		0.25*VDDIO	V	2
Rpu	Input pull-up resistance	40	85	190	KW	VDDIO=typ. Vinput=0V
Rpd	Input pull-down resistance	40	85	190	KW	VDDIO=typ. Vinput=3.3V
Outputs						
VOH(DC)	DC Output logic low voltage	0.85*VDDIO			V	VDDIO=min, IOH= - 2mA
VOL(DC)	DC Output logic high voltage			0.15*VDDIO	V	VDDIO=min, IOL= -2mA
Leakage						
IIN	Input leakage current (any input 0V<VIN<VDDIO)	-5		5	mA	**3**
IOZ	Tri-state output leakage current	-5		5	mA	**3**
IIN	Input leakage current (VIN=5.5V/0V) for 5V tolerant IO	-10		10	mA	**3**
IOZ	Tri-state output leakage current for 5V tolerant IO	-10		10	mA	**3**

Table 13 Electrical Characteristics of IO under 2.8V

AC&DC Electrical Characteristics and Operating Conditions of 1.8V Applications (JESD8-B)

Parameter	Description	Min.	Typ.	Max.	Unit	Note
Tc	Operating temperature	-40	25	125	°C	1
Freq	Maximum operating frequency			**100**	Mhz	1
VDD	Supply voltage of core power	**1.15**	**1.225**	**1.32**	V	1,**4**
VDDIO	Supply voltage of IO power	**1.62**	**1.8**	**1.98**	V	1
Tc	Operating temperature	-40	25	125	°C	1
Inputs						
VIH	Input logic low voltage	0.75*VDDIO		VDDIO+0.3	V	2
VIL	Input logic high voltage	-0.3		0.25*VDDIO	V	2
Rpu	Input pull-up resistance	70	150	320	KW	VDDIO=typ. Vinput=0V
Rpd	Input pull-down resistance	70	150	320	KW	VDDIO=typ. Vinput=3.3V
Outputs						
VOH(DC)	DC Output logic low voltage	0.85*VDDIO			V	VDDIO=min, IOH= - 2mA
VOL(DC)	DC Output logic high voltage			0.15*VDDIO	V	VDDIO=min, IOL= -2mA
Leakage						
IIN	Input leakage current (any input 0V<VIN<VDDIO)	-5		5	mA	**3**
IOZ	Tri-state output leakage current	-5		5	mA	**3**
IIN	Input leakage current (VIN=5.5V/0V) for 5V tolerant IO	-10		10	mA	**3**
IOZ	Tri-state output leakage current for 5V tolerant IO	-10		10	mA	**3**

Notation

1. Any target VDD must be specified along with VDDIO combinations separately. Maximum operating frequency and operating temperature should be included for different VDD/VDDIO conditions.
2. Please specify different types of input logic level for differnet types of pins (Data/Clock/Address/Commands). Please try to converge (summary) all input logic level in one specification.
3. Leakage sensitive applications (RTC, crystal pads) senstive to this specification. Co-simulation is needed.
4. Dynamic IR drop on VDD versus IO design window must be checked before tapeout

Table 14 Electrical Characteristics of IO under 1.8V

2.2.4 Storage Condition

1. Shelf life in sealed bag: 12 months at < 40℃ and < 90% relative humidity (RH).
2. After bag opened, devices subjected to infrared reflow, vapor-phase reflow, or equivalent processing must be:
   - A. Mounted within 168 hours at factory conditions of ≤ 30℃/60% RH, or
   - B. Stored at ≤ 20% RH
3. Devices require baking, before mounting, if:
   - A. 192 hours at 40℃ +5℃/-0℃ and < 5% RH for low temperature device containers, or

B. 24 hours at 125℃ +5℃/-0℃ for high temperature device containers.

2.2.5 AC Electrical Characteristics and Timing Diagram

2.2.5.1 External Memory Interface for LPDDR

External memory interface, shown in **Figure 4**, **Figure 5**, and **Figure 17**, is used to connect LPDDR device for MT6573. It includes the pins ED_CLK, ED_CLK_B, ECKE, ECS#, EWR#, ERAS#, ECAS#, EDQS[1:0], EA[15:0] and ED[15:0]. **Table 15** summarizes the symbol definition and the related timing specification.

LPDDR AC Timing Diagram

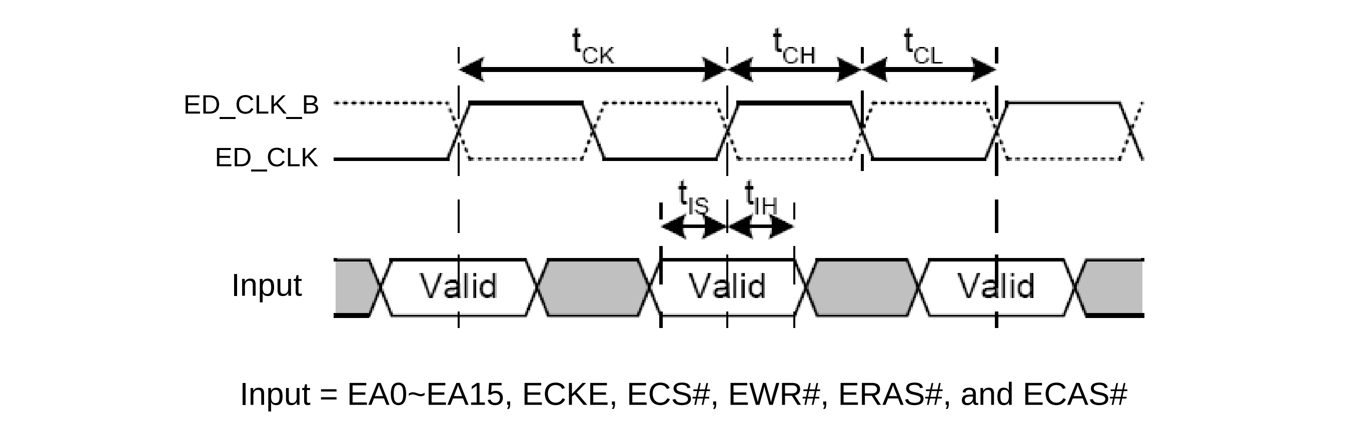


Figure 4 Basic Timing Parameter for LPDDR Commands

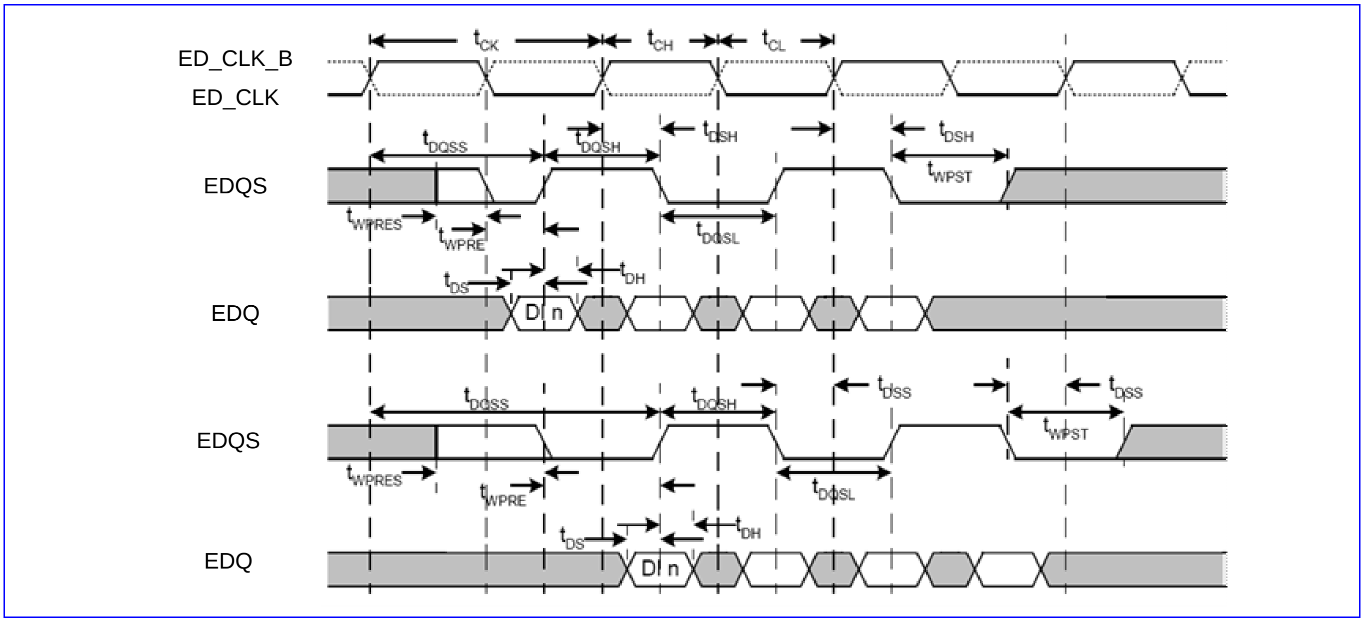


Figure 5 Basic Timing Parameter for LPDDR Write

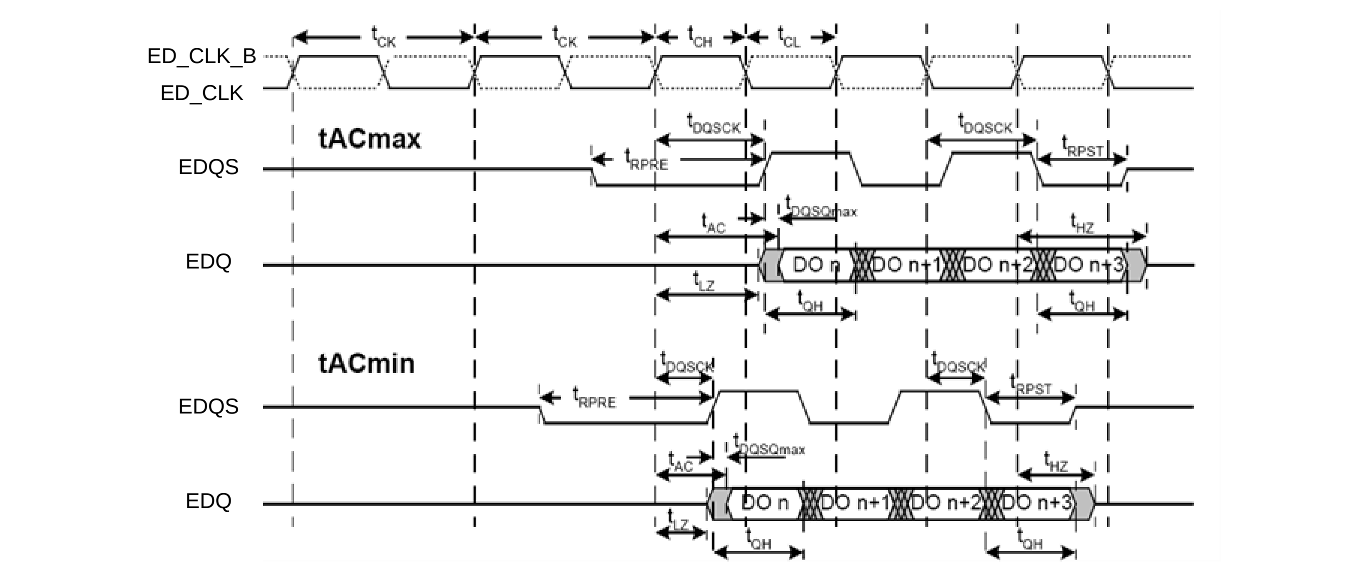


Figure 6 Basic LPDDR Read Timing Parameter

Symbol	Description	Min.	Typ.	Max.	Unit
tAC[1]	DQ output access time from CK/CK'	2.0		6.5	ns
tDQSCK[1]	DQS output access time from CK/CK'	2.0		6.5	ns
tCK	Clock cycle time	9.6			ns
tCH	Clock high level width	0.45		0.55	tCK
tCL	Clock low level width	0.45		0.55	tCK
tHP	Clock half period	0.45		0.55	tCK
tDS	DQ & DM input setup time	0.9			ns
tDH	DQ & DM input hold time	0.9			ns
tIS	Address & control input setup time	1.5			ns
tIH	Address & control input hold time	1.5			ns
tLZ[1]	DQ & DQS low-impedance time from CK/CK'	1.0			ns
tHZ[1]	DQ & DQS high-impedance time from CK/CK'			6.5	ns
tDQSQ[1]	DQS-DQ skew			0.6	ns
tQH[1]	DQ/DQS output hold time from DQS	tHP-tQHS			
tDQSH	DQS input high-level width	0.4			tCK
tDQSL	DQS input low-level width	0.4			tCK
tMRD[2]	MODE register set command period	2			tCK
tRPRE[1]	Read preamble	0.9		1.1	tCK
tRPST[1]	Read postamble	0.4		0.6	tCK
tRAS[2]	ACTIVE to PRECHARGE command period	4		11	tCK
tRC[2]	ACTIVE to ACTIVE command period	8		15	tCK
tRFC[2]	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	8		23	tCK
tRCD[2]	ACTIVE to READ or WRITE delay	2		5	tCK
tRP[2]	PRECHARGE command period	2		5	tCK
tRRD[2]	ACTIVE bank A to ACTIVE bank B delay	2		3	tCK
tWR[2]	WRITE recovery time	2		3	tCK
tWTR[2]	Internal write to READ command time	1		2	tCK
tXSR[2]	SELF REFRESH exit to next valid command	0		31	tCK
tXP[2]	EXIT power down to next valid command delay	1		8	tCK
tCKE[2]	CKE min. pulse width (high & low pulse width)	2		2	tCK
tREF[2]	Refresh Period	10		8192	tCK

Table 15 The LPDDR AC timing parameter table of external memory interface

2.3 System Configuration

2.3.1 Strapping Resistors

Pin Name	Description
KCOL1	Pull-up with 2M ohm resistor: NAND boot mode

Table 16 Strapping Table

2.3.2 Mode Selection

Pin Name	Description
KCOL0	0: Trigger USB download 1: NA
KCOL1	0: NOR boot 1: NAND boot
KROW0	0: Trigger USB download without battery 1: NA

Table 17 Mode Selection of Chip

2.3.3 Constant Tied Pins

Pin Name	Description
PMU_TESTMODE	PMU test mode enable (tie to GND)
TESTMODE	Test mode (tie to GND)
FSOURCE_P	EFUSE burning (tie to GND)
ICORE	Test mode control (tie to GND)

2.4 Power on Sequence

The power-on/off sequence which is controlled by “Control” and “Reset Generator” is shown as follows,

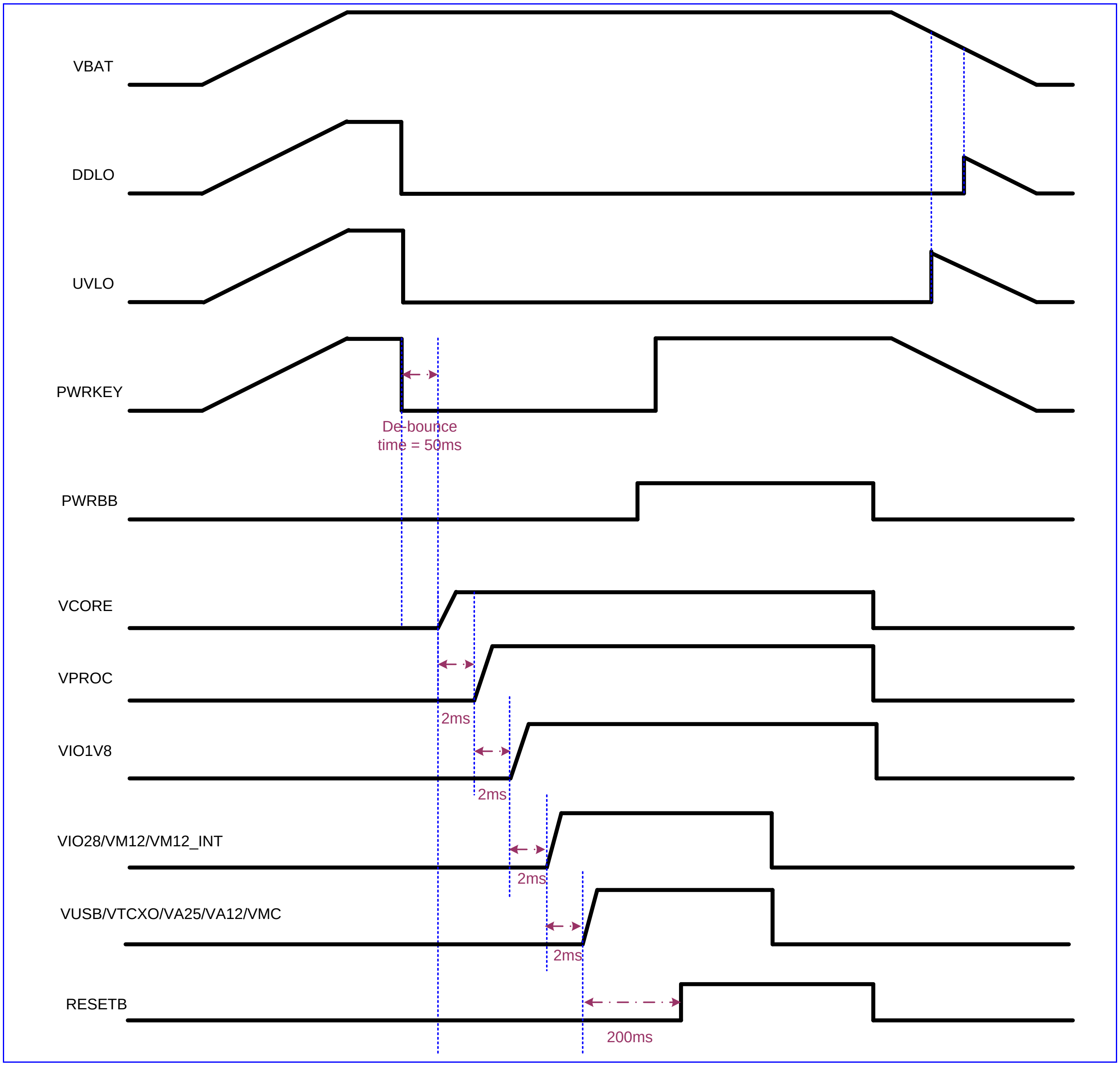


Figure 7 Power-on/off Control Sequence

Note that the above figure only shows one power-on/off condition. The MT6573 handles the powering ON and OFF of the handset. The following three different ways can switch-on the handset (When VBAT>=3.2V):

- Pulling PWRKEY low (User push PWRKEY)
- Pulling PWRBB high (Baseband BB_WakeUp)
- Valid charger plug-in

Pulling PWRKEY low is a normal way to turn on the handset. That will turn on VCORE, VPROC, VIO1V8, VIO28/VM12/VM12_INT and VUSB/VTCXO/VA25/VA12/VMC as long as the PWRKEY is kept low. The microprocessor then starts and pulls PWRBB high. After that PWRKEY can be released. Pulling PWRBB high will also turn on the handset. This is the case when the alarm in the RTC expires.

Besides, applying a valid external supply on CHRIN will also turn on the handset. However, If the battery is in UV state (VBAT<3.2V), the handset can't be turned-on in any way.

The UVLO function in the MT6573 prevents system startup when initial voltage of the main battery is below the 3.2V threshold. When the battery voltage is greater than 3.2V, the UVLO comparator switches and the threshold is reduced to 2.9V. This allows the handset to start smoothly unless the battery decays to 2.9V and below.

Once the MT6573 enters UVLO state, it draws very low quiescent current. The VRTC LDO is still active until the DDLO disables it.

2.5 Analog Baseband

2.5.1 Audio Mixed-Signal Blocks

2.5.1.1 Block Descriptions

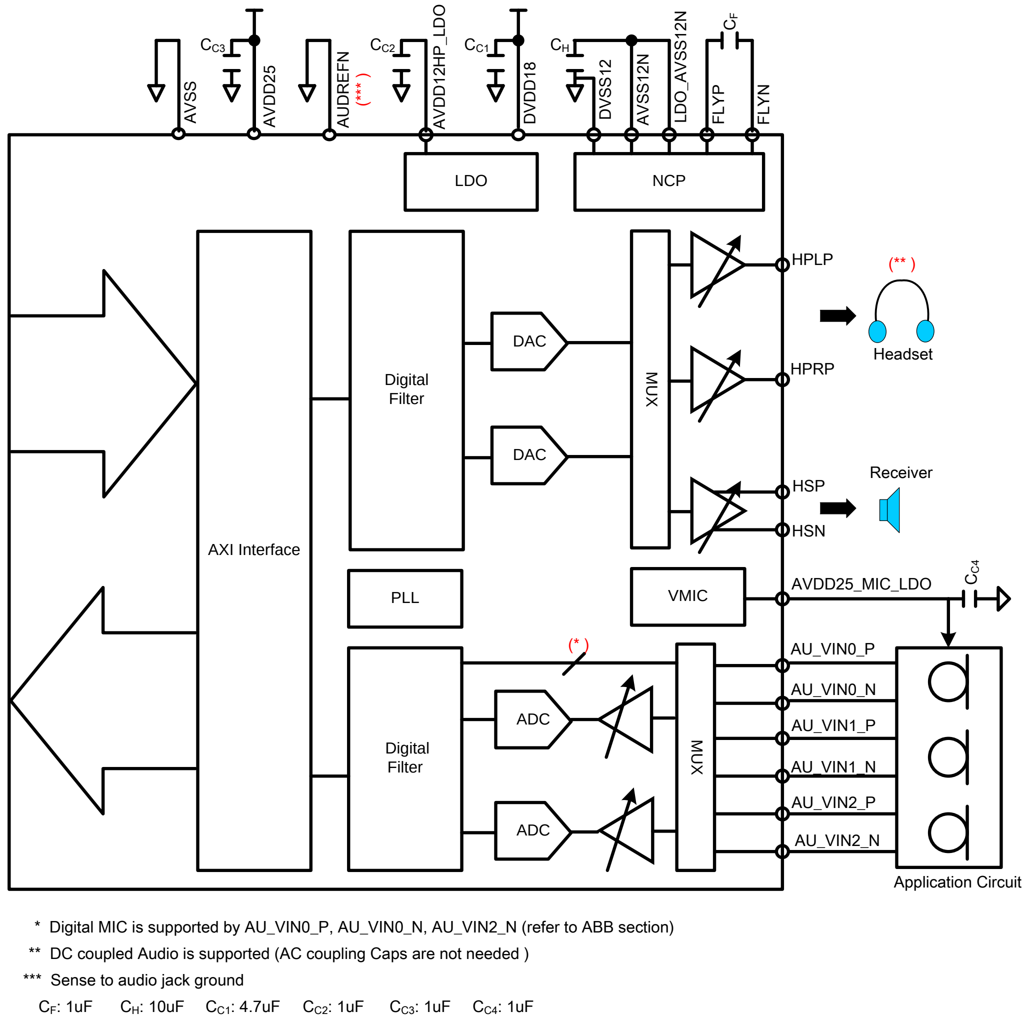


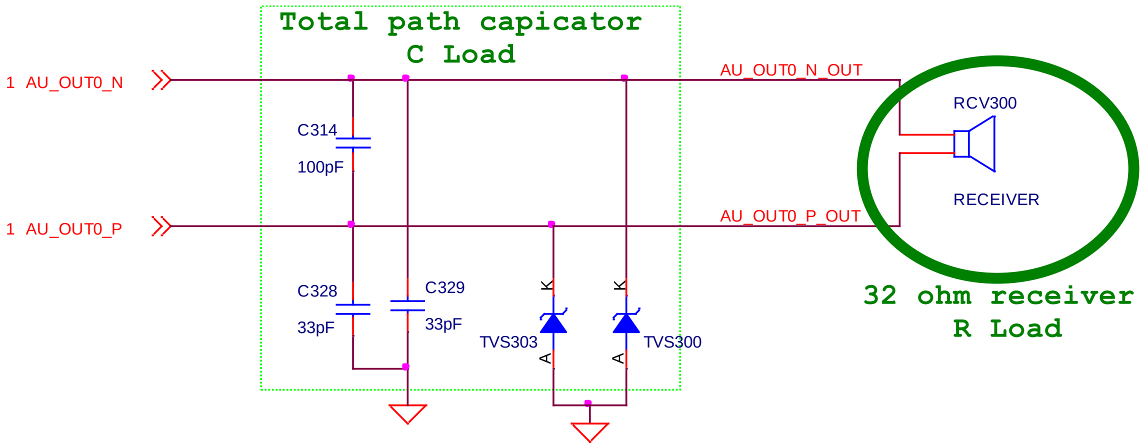
Figure 8 Block Diagram of Audio/Speech Part

2.5.1.2 Functional Specification

The following table gives functional specifications of voice-band uplink/downlink blocks.

Symbol	Description	Min.	Typ.	Max.	Unit
VAUDP	Analog positive power supply (AVDD12HP_LDO)		1.25		V
VAUDN	Analog negative power supply (AVSS12N)		-1.25		V
AVDD	Analog Power Supply (AVDD25)	2.4	2.5	2.6	V
VMIC	Microphone Biasing Voltage		2.5		V
Uplink Path					
SINAD	Signal to Noise and Distortion Ratio Input Level: -40 dbm0 Input Level: 0 dbm0	29	69		dB dB
RIN	Input Impedance (Differential)	13	20	27	KΩ
Downlink Path					
SINAD	Signal to Noise and Distortion Ratio Input Level: -40 dBm0 Input Level: 0 dBm0	29	69		dB dB
RLOAD	Output Resistor Load (Differential)	28			Ω
CLOAD	Output Capacitor Load			200	pF

Table 18 Functional specifications of analog voice blocks



Functional specifications of the audio blocks are described in the following.

Symbol	Description	Min.	Typ.	Max.	Unit
Fs	Sampling Rate	32	44.1	48	KHz
AVDD	Power Supply (AVDD25)	2.4	2.5	2.6	V
PSNR	Peak Signal to Noise Ratio		88		dB
VOUT	Output Swing for 0dBFS Input Level		0.5		Vrms

THD	Total Harmonic Distortion 22mW at 32 Ω Load			-70	dB dB
RLOAD	Output Resistor Load (Single-Ended)	32			Ω
CLOAD	Output Capacitor Load			200	pF

Table 19 Functional specifications of the analog audio blocks

2.5.2 BBRX/TX

2.5.2.1 BBRX Functional Specification

The receiver (RX) performs base-band I/Q channels downlink analog-to-digital conversion:

1. *Analog input multiplexer:* For each channel, a 4-input multiplexer that supports offset and gain calibration is included.
2. *A/D converter:* Two high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.

The functional specifications of the base-band downlink receiver are listed in the following table.

Symbol	Parameter	Min	Typical	Max	Unit
V_{CM}	Common Mode Input Voltage	1.08	1.2	1.32	V
V_{IN}	Differential Analog Input Voltage (Peak-to-Peak)			4	V
fs	Input Clock Frequency - Clock Rate (WCDMA & TD-SCDMA) - Clock Rate (GSM)		245.76 208		MHz MHz
	Input clock Duty Cycle	49.5	50	50.5	%
	RMS Input clock Period Jitter, WCDMA & TD-SCDMA configurations[1]			0.14	%
	RMS Input Clock Period Jitter, GSM configuration[2]			0.61	%
V_{AVDD25}	Analog Power Supply Voltage	2.4	2.5	2.6	V
V_{AVDD12}	Digital Power Supply Voltage	1.2	1.25	1.3	V
T_J	Junction Temperature	-40	25	125	℃
Performance					
V_{LSB}	LSB Voltage		3.232		V
R_{IN}	Differential Input Resistance	20	32.5	45	kΩ
C_{IND}	Differential Input Capacitance				pF
C_{INC}	Common Mode Input Capacitance				pF
V_{OS}	Differential Input-Referred Offset			10	mV
I_{CM}	Common Mode Input Current Magnitude			1	uA

	Signal to In-Band Noise, WCDMA configuration[3]	76	79		dB
	Signal to In-Band Noise, TD-SCDMA configuration[4]	82	85		dB
	Signal to In-Band Noise, GSM configuration[5]	88	91		dB
	IM3 distortion, 10.08MHz & 20.4MHz input[6]			-78	dB
	IM3 distortion, 3.5MHz & 5.9MHz input[7]			-78	dB
	IM2 distortion, 4.88MHz & 5.12MHz input[8]			-78	dB
	IM2 distortion, 14.88MHz & 15.12MHz input[9]			-78	dB
	AVDD25 Analog Supply Current(Active, per channel)		1.1	1.4	mA
	AVDD12 Analog Supply Voltage(Active, per channel)		0.7	0.8	mA
	AVDD12 Analog Supply Current(Idle 80 degC, per channel)			<1	uA
	AVDD12 Analog Supply Voltage(Idel, 125 degC, per channel)			<3	uA

[1] The input clock jitter specification is based on a fractional-N jitter model.
The specification is not valid for Gaussian jitter. Maximum Gaussian jitter would be lower.

[2] The input clock jitter specification is based on an integer-N jitter model.
The specification is not valid for Gaussian jitter. Maximum Gaussian jitter would be lower.

[3] The test signal for performance measurement is a 4 V-pp differential 2.8 MHz sine wave.
In-Band noise is total noise contained in the 100 Hz to 1.92 MHz band.

[4] The test signal for performance measurement is a 4 V-pp differential 1.6 MHz sine wave.
In-Band noise is total noise contained in the 100 Hz to 640 kHz band.

[5] The test signals for performance measurement is a 4 V-pp differential 200 kHz sine wave.
In-Band noise is total noise contained in the 217 Hz to 135 kHz band.

[6] The test signal for performance measurement consists of a 144 mV V-pp differential 10.08 MHz sine wave and a 18 mV V-pp differential 20.4 MHz sine wave.
The IM3 distortion is at 240 kHz.

[7] The test signal for performance measurement consists of a 633 mV V-pp differential 3.5 MHz sine wave and a 132 mV V-pp differential 5.9 MHz sine wave.
The IM3 distortion is at 1.1 MHz.

[8] The test signal for performance measurement consists of a 320 mV V-pp differential 4.88 MHz sine wave and a 320 mV V-pp differential 5.12 MHz sine wave.
The IM2 distortion is at 240 kHz.

[9] The test signal for performance measurement consists of a 100 mV V-pp differential 14.88 MHz sine wave and a 100 mV V-pp differential 15.12 MHz sine wave.
The IM2 distortion is at 240 kHz.

Table 20 Base-band Uplink Transmitter Specifications

2.5.2.2 Functional Specification

The transmitter (TX) performs base-band I/Q channels up-link digital-to-analog conversion. Each channel includes:

1. *11-Bits D/A Converter:* It converts digital 8PSK/WCDMA modulated signals to analog domain. The input to the DAC is sampled at 61.44MHz/26MHz/(3G/2G) rate with 11-bits resolution.
2. *Smoothing Filter:* The low-pass filter performs smoothing function for DAC output signals with a 9MHz/1.8MHz (3G/2G) 2nd-order Butterworth frequency response.

Symbol	Description	Min.	Typ.	Max.	Unit
N	Resolution		11		Bit
FS	Sampling Rate (3G/2G)		61.44/26		MSPS
SINAD	Signal to Noise and Distortion Ratio 3G 2G	 55 65	 60 70		 dB dB
	Output Swing	0.9	1	1.1	V
VOCM	Output CM Voltage	1.15 1.05	1.2 1.1	1.25 1.15	V V
	Output Capacitance			20	PF
	Output Resistance		1.5		KΩ
DNL	Differential Nonlinearity		+/- 0.5		LSB
INL	Integral Nonlinearity		+/- 1.0		LSB
OE	Offset Error		+/- 1		mV
FSE	Full Swing Error		+/- 30		mV
FCUT	Filter –3dB Cutoff Frequency 3G 2G		 9 1.8		 MHz MHz
ATT	Filter Attenuation (3G) at 1.92-MHz 12.5-MHz 40.0-MHz Filter Attenuation (2G) at 100-KHz 270-KHz 4.33-MHz		 0.02 5.6 28 0 0.005 15		 dB dB dB dB dB dB
	I/Q Gain Mismatch		+/- 0.1		dB
	I/Q Phase Mismatch		+/- 1.0		deg
EVM	WCDMA Modulation		0.25	0.4	%
ACLR1	ACLR1 (WCDMA modulation 5MHz offset)		-65	-60	dB
ACLR2	ACLR2 (WCDMA modulation 10MHz offset)		-70	-65	dB
	Out-of-Band Noise Density (WCDMA) 7.5M-12.5M 12.5M-40M		 -140 -145	 -135 -140	 dBc/Hz dBc/Hz

	> 40MHz		-160	-155	dBc/Hz
DVDD	Digital Power Supply	1.1	1.2	1.3	V
AVDD	Analog Power Supply	2.4	2.5	2.6	V
T	Operating Temperature	-20		80	℃
	Current Consumption Power-up Power-Down		 9.4/5 1		 mA μA

Table 21 Base-band Uplink Transmitter Specifications

2.5.3 Auxiliary ADC / Touch Screen Controller

2.5.3.1 Block Descriptions

Auxiliary ADC serves as not only measuring ADC but also the resistive touch panel controller. The auxiliary ADC includes the following functional blocks:

1. *Analog Multiplexer:* The analog multiplexer selects signal from one of the auxiliary input channels. There are 16 input channels of AuxADC. Some are for internal voltage measuring and some for external voltage measuring. Real world message to be monitored, like temperature, should be transferred to the voltage domain.
2. *12 bits A/D Converter:* The ADC converts the multiplexed input signal to 12-bit digital data.

Touch Screen controller can drive external touch panel via Pads XP, XM, YP, and YM and AuxADC as a voltage meter can obtain X/Y-position of touched point on the external touch screen. Touch Screen Interface contains three main blocks. They are touch screen pads control logic, ADC interface logic and interrupt generation logic. Touch Screen Interface supports two conversion modes: separate X/Y position conversion mode and auto (sequential) X/Y position conversion mode.

For brief description of AuxADC input channels, please refer to Table 25.

AuxADC Channel ID	Description
Channel 0	Vbat
Channel 1	Isense
Channel 2	CHRIN
Channel 3	Tsense
Channel 4	External (AUXADC4)
Channel 5	External (AUXADC5)
Channel 6	External (AUXADC6)
Channel 7	External (AUXADC7)
Channel 8	External (AUXADC8)
Channel 9	NA
Channel 10	NA

AuxADC Channel ID	Description
Channel 11	NA
Channel 12	NA
Channel 13	XP (Touch Panel)
Channel 14	YP (Touch Panel)
Channel 15	YM (Touch Panel)

Table 22 AuxADC channel list

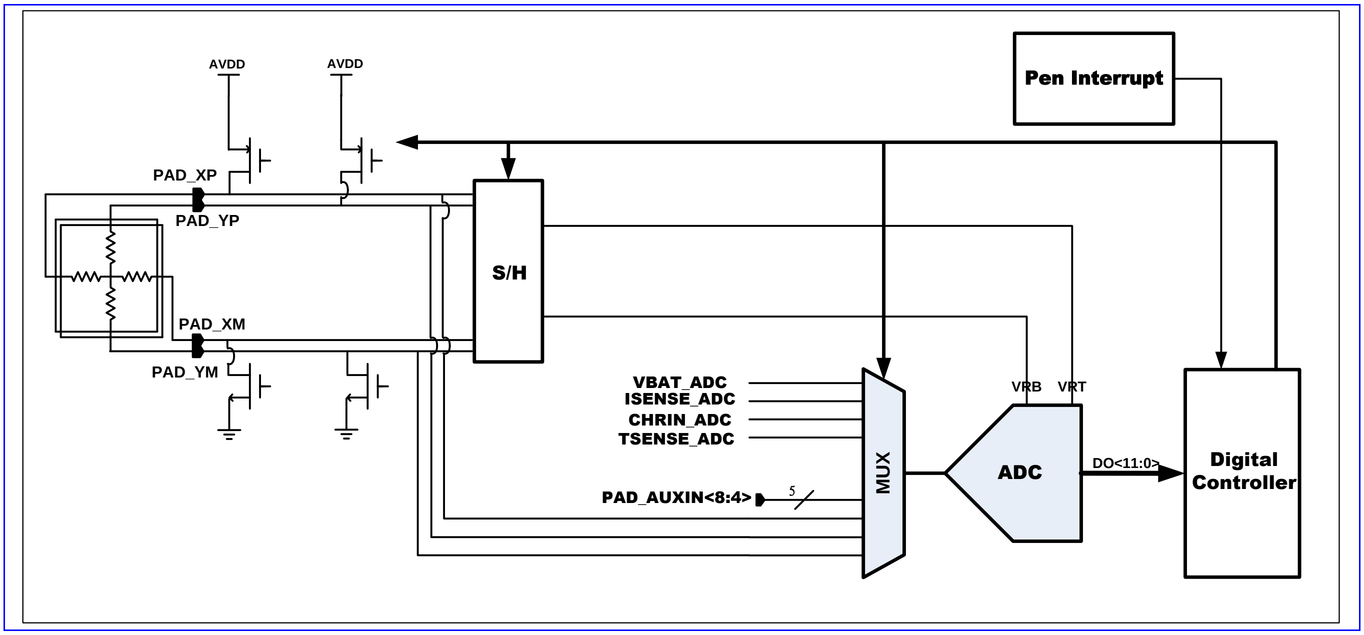


Figure 9 Block diagram of AuxADC and Touch Screen Interface

2.5.3.2 Function Specifications

The functional specifications of the auxiliary ADC are listed in the following table.

Symbol	Description	Min.	Typ.	Max.	Unit
N	Resolution		12		Bit
FC	Clock Rate		3.84		MHz
FS	Sampling Rate @ N-Bit		3.84/(N+4)		MSPS
	Input Swing	0		AVDD	V
CIN	Input Capacitance Unselected Channel Selected Channel			50 4	fF pF
RIN	Input Resistance				

	Unselected Channel Selected Channel	400 1			MΩ MΩ
	Clock Latency		N+4		1/FC
DNL	Differential Nonlinearity		+1.0/-1.0		LSB
INL	Integral Nonlinearity		+2.0/-2.0		LSB
OE	Offset Error (without calibration)		+/- 10		mV
FSE	Full Swing Error (without calibration)		+/- 10		mV
SINAD	Signal to Noise and Distortion Ratio (10-KHz Full Swing Input & 13-MHz Clock Rate)	62	68		dB
DVDD	Digital Power Supply	1.1	1.2	1.3	V
AVDD	Analog Power Supply	2.4	2.5	2.6	V
T	Operating Temperature	-20		80	℃
	Current Consumption Power-up Power-Down		 280 1		 μA μA
Ztp	Supported Touch Panel Impedance	200		2K	Ohm

Table 23 The Functional specification of Auxiliary ADC

2.5.4 Phase Locked Loop

2.5.4.1 Block Descriptions

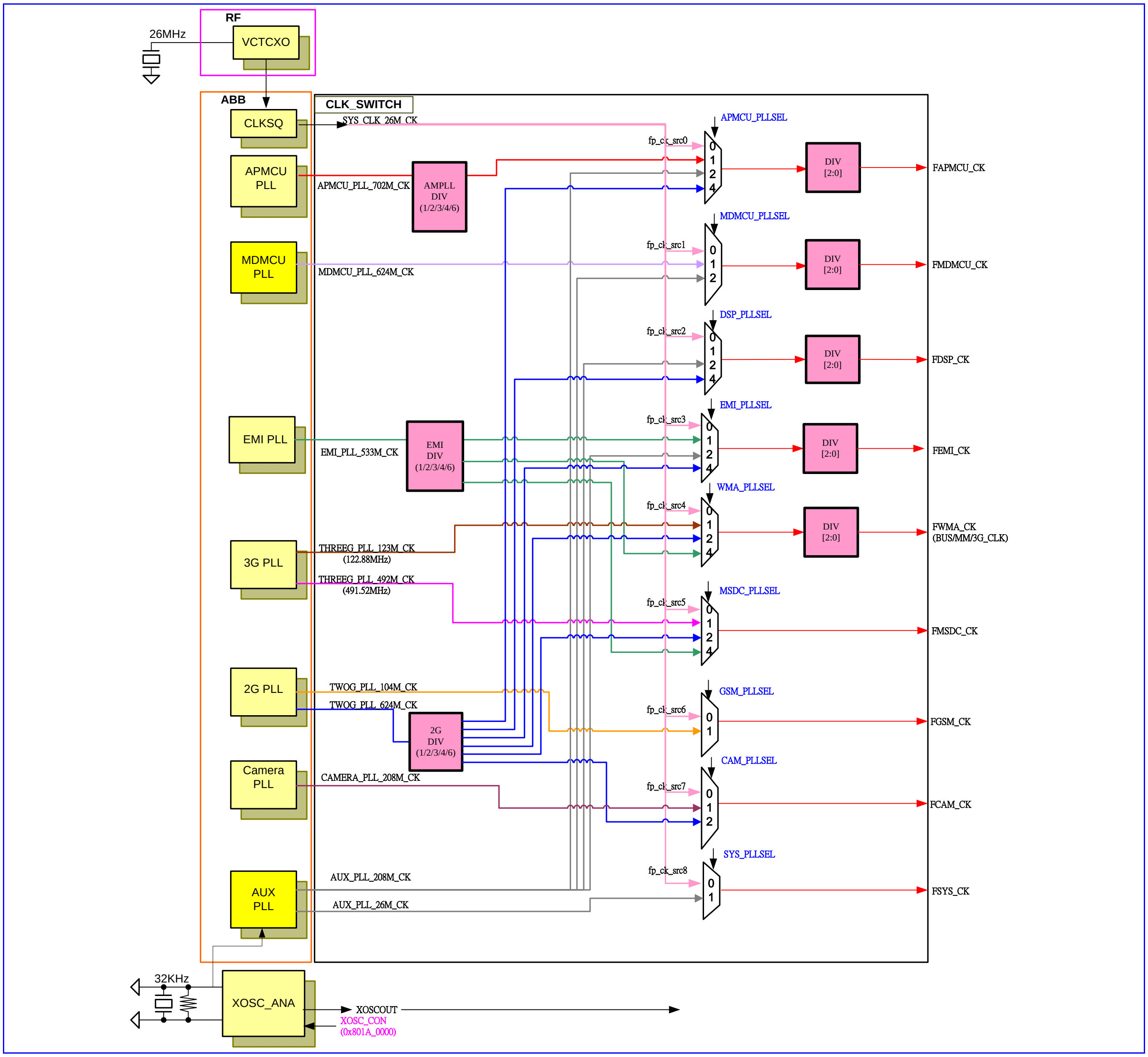


Figure 10 Block diagram of clock tree

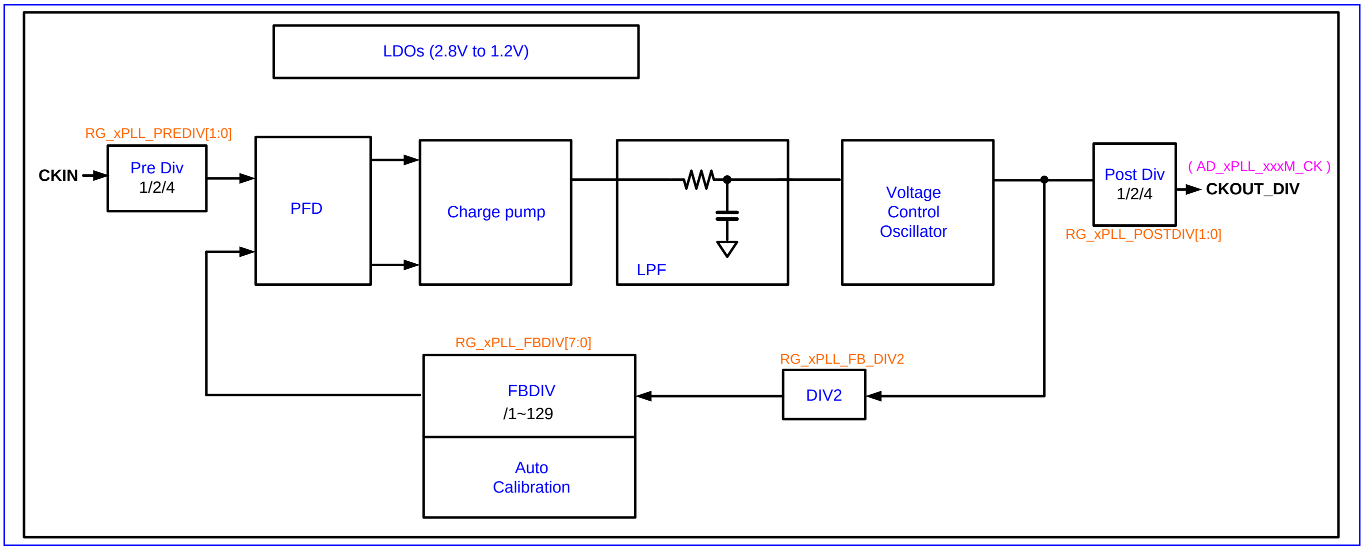


Figure 11 Block diagram of PLL

2.5.4.2 Function Specifications (TBD)

The functional specification of MCU PLL is shown in the following table. **(Note: list spec tables of all PLL)**

Symbol	Description	Min.	Typ.	Max.	Unit
Fin	Input Clock Frequency		2		MHz
Fout	Output Clock Frequency	13		702	MHz
	Min. output frequency step		13		MHz
	Settling Time for power on For band switching		 TBD 9		us
	Output Clock Duty Cycle	TBD	48/52	TBD	%
	Output Clock Jitter		55ps		ps
DVDD	Digital Power Supply	1.0	1.2	1.4	V
AVDD	Analog Power Supply	2.4	2.5	2.6	V
T	Operating Temperature	-20		80	℃
	Current Consumption For AVDD For DVDD		 TBD TBD		mA
	Power Down Current Consumption For AVDD For DVDD			 TBD TBD	uA

Table 24 The Functional Specification of MCU PLL

2.5.5 Clock Squarer

2.5.5.1 Block Descriptions

For most VCXO, the output clock waveform is sinusoidal with too small amplitude (about several hundred mV) to make MT65xx digital circuits function well. Clock squarer is designed to convert such a small signal to a rail-to-rail clock signal with excellent duty-cycle. It provides also a pull-down function when the circuit is powered-down.

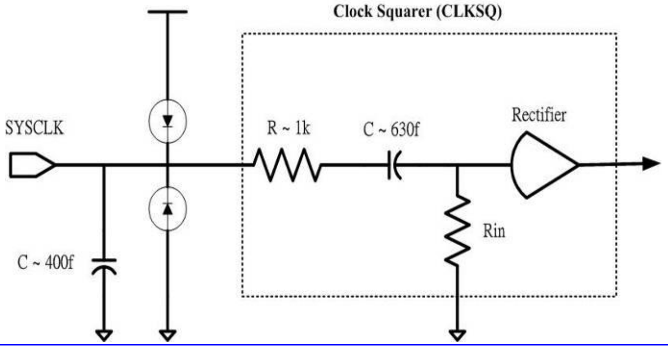


Figure 12 Equivalent circuit of Clock Squarer.

2.5.5.2 Function Specifications

The functional specification of clock squarer is shown in Table 12.

Symbol	Description	Min.	Typ.	Max.	Unit
Fin	Input Clock Frequency	13	26		MHz
Fout	Output Clock Frequency	13	26		MHz
Vin	Input Signal Amplitude		500	AVDD	mVpp
DcycIN	Input Signal Duty Cycle		50		%
DcycOUT	Output Signal Duty Cycle	DcycIN-5		DcycIN+5	%
TR	Rise Time on Pin CLKSQOUT			5	ns/pF
TF	Fall Time on Pin CLKSQOUT			5	ns/pF
DVDD	Digital Power Supply	1.1	1.2	1.3	V
AVDD	Analog Power Supply	1.1	1.2	1.3	V
T	Operating Temperature	-20		80	℃
	Current Consumption		100		uA

Table 25 Functional Specification of Clock Squarer

2.5.6 32-KHz Crystal Oscillator (RTC)

The low-power 32-KHz crystal oscillator XOSC32 is designed to work with an external piezoelectric 32.768KHz crystal and a load composed of two functional capacitors, as shown in the following figure.

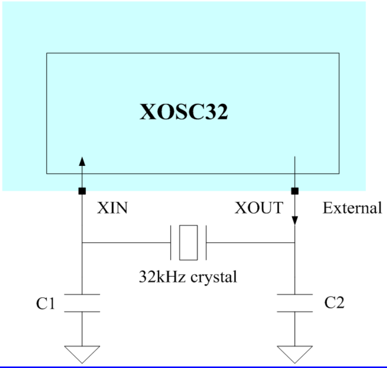


Figure 13 Block diagram of XOSC32

The functional specification of XOSC32 is shown in the following table.

Symbol	Description	Min.	Typ.	Max.	Unit
AVDDRTC	Analog power supply	1.0	2.8	3.0	V
Tosc	Start-up time			1	sec
Dcyc	Duty cycle	35	50		%
	Current consumption		5	10	µA
T	Operating temperature	-20		80	℃

Table 26 Functional Specification of XOSC32

Here below are a few recommendations for the crystal parameters for use with XOSC32.

Symbol	Description	Min.	Typ.	Max.	Unit
F	Frequency range		32768		Hz
GL	Drive level			5	uW
Δf/f	Frequency tolerance		+/- 20		ppm
ESR	Series resistance			50	KΩ
C0	Static capacitance		0.9		pF
CL[3](C1/C2in the figure)	Load capacitance		12.5		pF

Table 27 Recommended Parameters of the 32KHz crystal

2.5.7 APC DAC

2.5.7.1 Block Descriptions

The APC-DAC is a 10-bits DAC with output buffer aimed for automatic power control. Here blow are its analog pin assignment and functional specification tables.

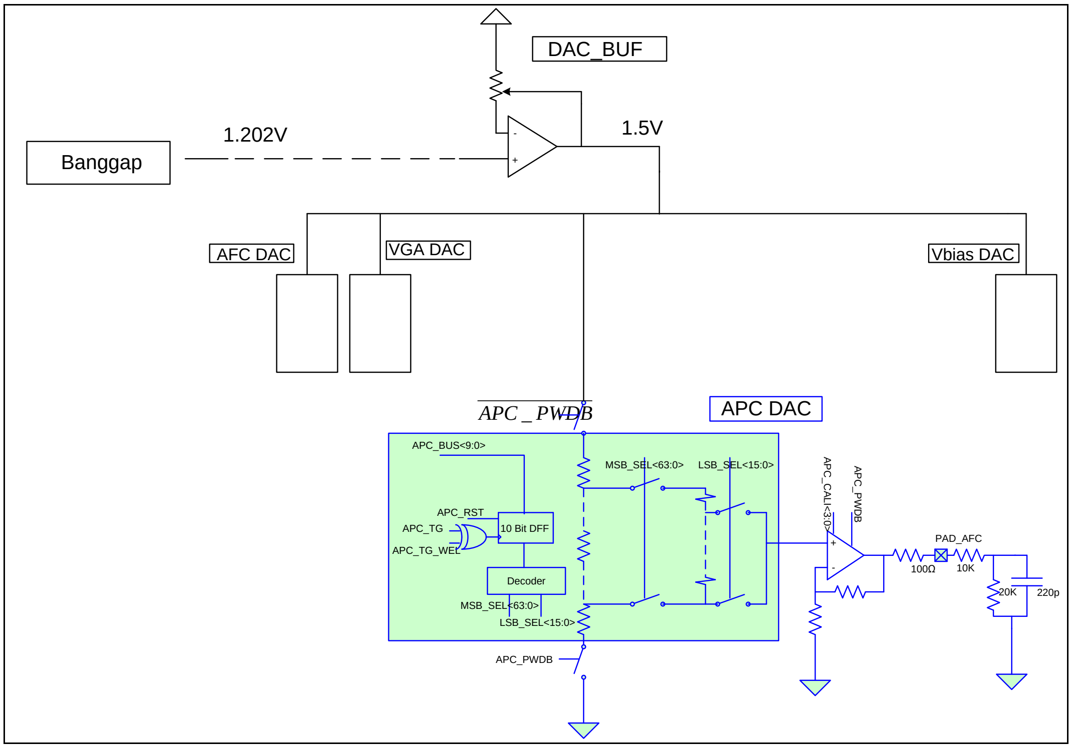


Figure 14 Block diagram of XOSC32

2.5.7.2 Function Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
FS	Sampling Rate			1.0833	MSPS
SINAD	Signal to Noise and Distortion Ratio (10-KHz Sine with 1.0V Swing & 100-KHz BW)		50		dB
	99% Settling Time (Full Swing on Maximal Capacitance)			5	μS
	Output Swing	0		AVDD	V

	Output Capacitance		200	2200	pF
	Output Resistance	0.47	10		KΩ
DNL	Differential Nonlinearity for code 20 to 970		+/- 0.5		LSB
INL	Integral Nonlinearity for code 20 to 970		+/- 1.0		LSB
PSRR	Power supply ripple rejection ratio	47			dB
DVDD	Digital Power Supply	1.1	1.2	1.3	V
AVDD	Analog Power Supply	2.5	2.8	3.1	V
T	Operating Temperature	-20		80	℃
	Current Consumption Power-up Power-Down		 300 	 1	 μA μA

Table 28 APC-DAC Specifications

2.5.8 AFC DAC

2.5.8.1 Block Descriptions

As shown in the following figure, AFC-DAC is designed to produce a single-ended output signal at AFC pin. AFC pin should be connected to an external 1st-order R-C low pass filter to meet the 13-bits resolution (DNL) requirement[4].

[4] DNL performance depends on external output RC filter bandwidth: the narrower the bandwidth, the better the DNL. Thus, there exists a tradeoff between output setting speed and DNL performance

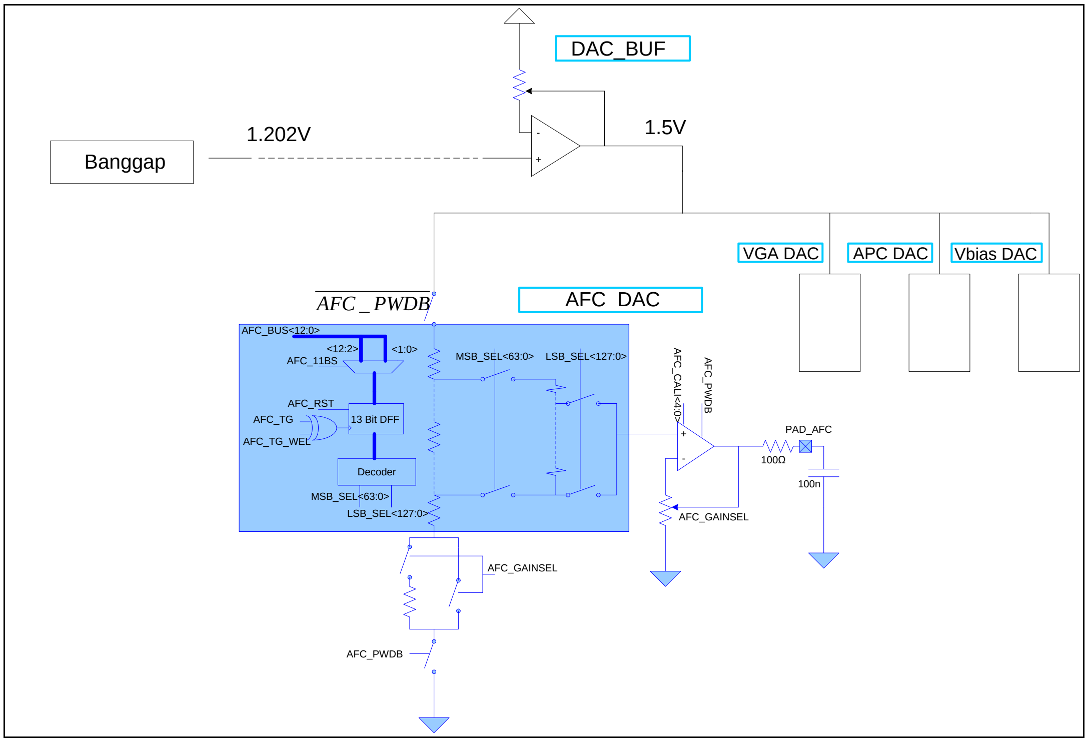


Figure 15 Block diagram of XOSC32

2.5.8.2 Functional Specifications

The following table gives the electrical specification of AFC-DAC.

Symbol	Description	Min.	Typ.	Max.	Unit
N	Resolution		13		Bit
FS	Sampling Rate			1083	KHz
DVDD	Digital Power Supply	1	1.2	1.4	V
AVDD	Analog Power Supply	2.5	2.8	3.1	V
T	Operating Temperature	-20	60	125	℃
	Current Consumption Power-up Power-Down		 400 	 1	 μA μA
	Output Range Gainsel=0 Gainsel=1		 AVDD/2±3/8*AVDD 0~AVDD		V
	Output Resistor (in AFC output RC network)		100		Ω
DNL	Differential Nonlinearity		+1/-1		LSB

	Code 0~8192, after RC filter, output voltage 0.35~2.45V(gainsel=0)				
INL	Integral Nonlinearity Code 0~8192, after RC filter, output voltage 0.35~2.45V(gainsel=0)		+5/-5		LSB
	Settling time		166		µs
	Maximum code difference		70		LSB
PSR	Power supply ripple rejection ratio	47			dB

Table 29 AFC-DAC Specifications

2.5.9 Video DAC (TVDAC)

The 10bit Video DAC transforms the digital composite video signal (NTSC/PAL) to analog signal. Here below are its functional specification tables.

Symbol	Description	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
FS	Sampling Rate		27		MSPS
	Output Current		26.67	35	mA
	Output Loading Resistance		37.5		Ω
DNL	Differential Nonlinearity[1]		+/- 1		LSB
INL	Integral Nonlinearity		+/- 2		LSB
DVDD	Digital Power Supply	1.1	1.2	1.3	V
AVDD	Analog Power Supply	2.5	2.8	3.1	V
T	Operating Temperature	-20		80	℃
	Current Consumption Power-up Power-Down		 35 	 1	 mA µA

Table 30 TV DAC Specifications

2.5.10 MIPI

Consult the *MIPI Camera Interface Specification (CSI-2 V1.0) and Display Interface Specification(DSI, DPI-2,*

DPI-2, please see http://www.mipi.org/specifications) for more information on MIPI usage and requirements.

2.5.11 USB2.0

Consult the *Universal Serial Bus Specification*, Revision 2.0 (see www.usb.org/developers) for more information on USB usage and requirements.

2.6 Power Management Unit

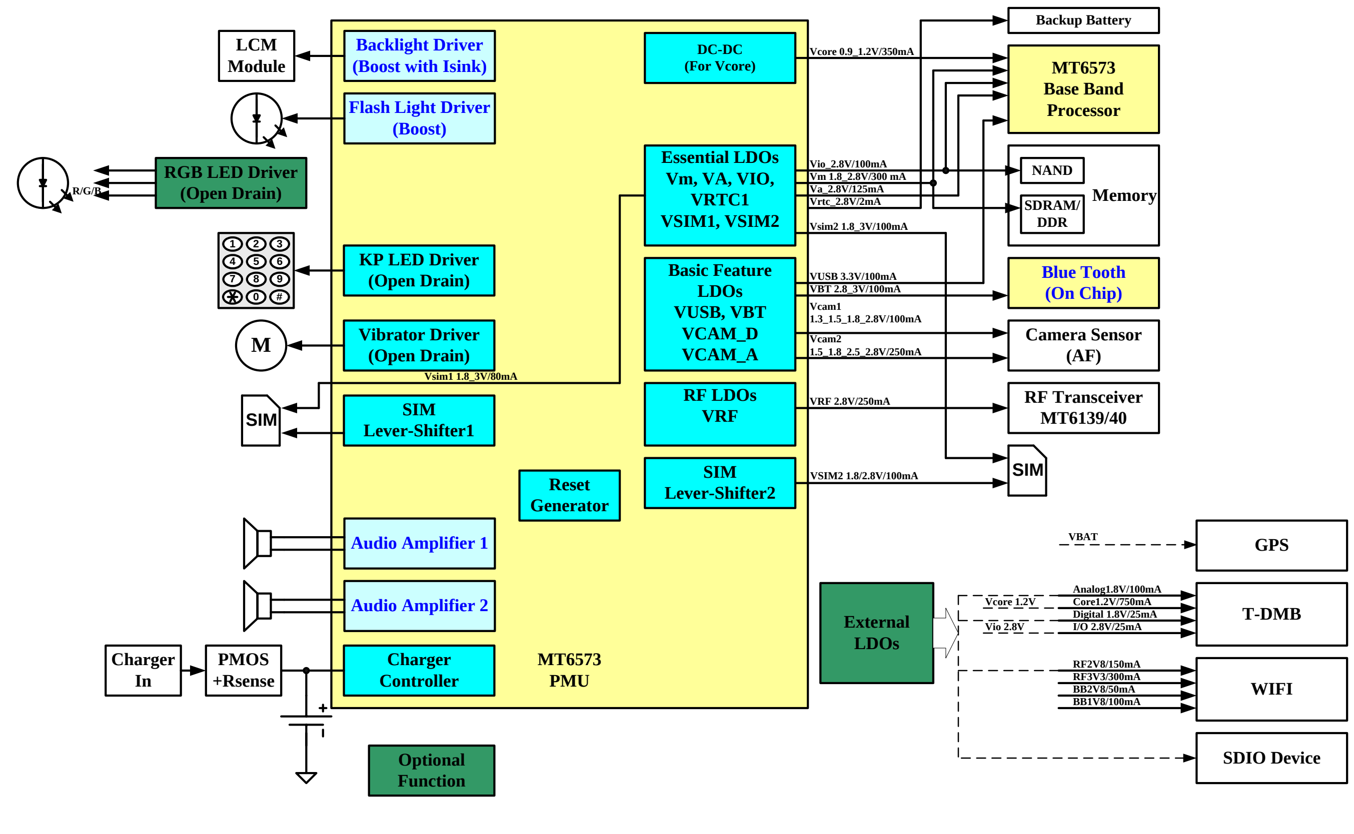


Figure 16 PMU system block diagram

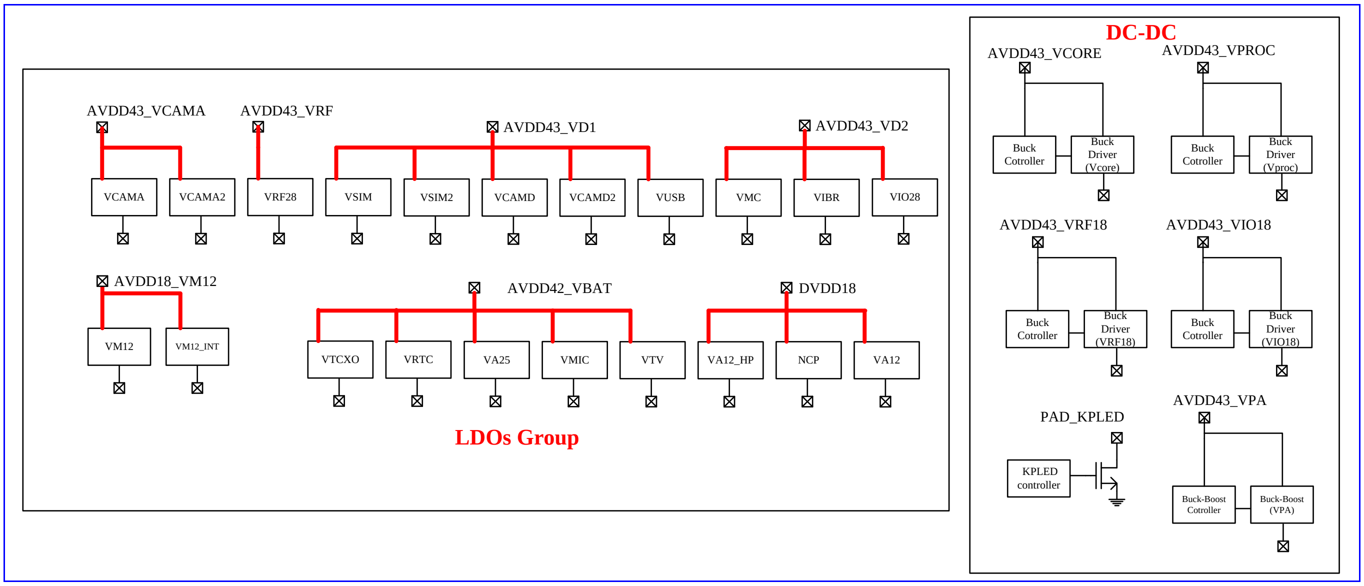


Figure 17 Power domain

2.6.1 Low Dropout Regulators (LDOs), Buck Converter and Reference

The PMU Integrates 12 LDOs that are optimized for their given functions by balancing quiescent current, dropout voltage, line/load regulation, ripple rejection, and output noise.

2.6.1.1 Block Description

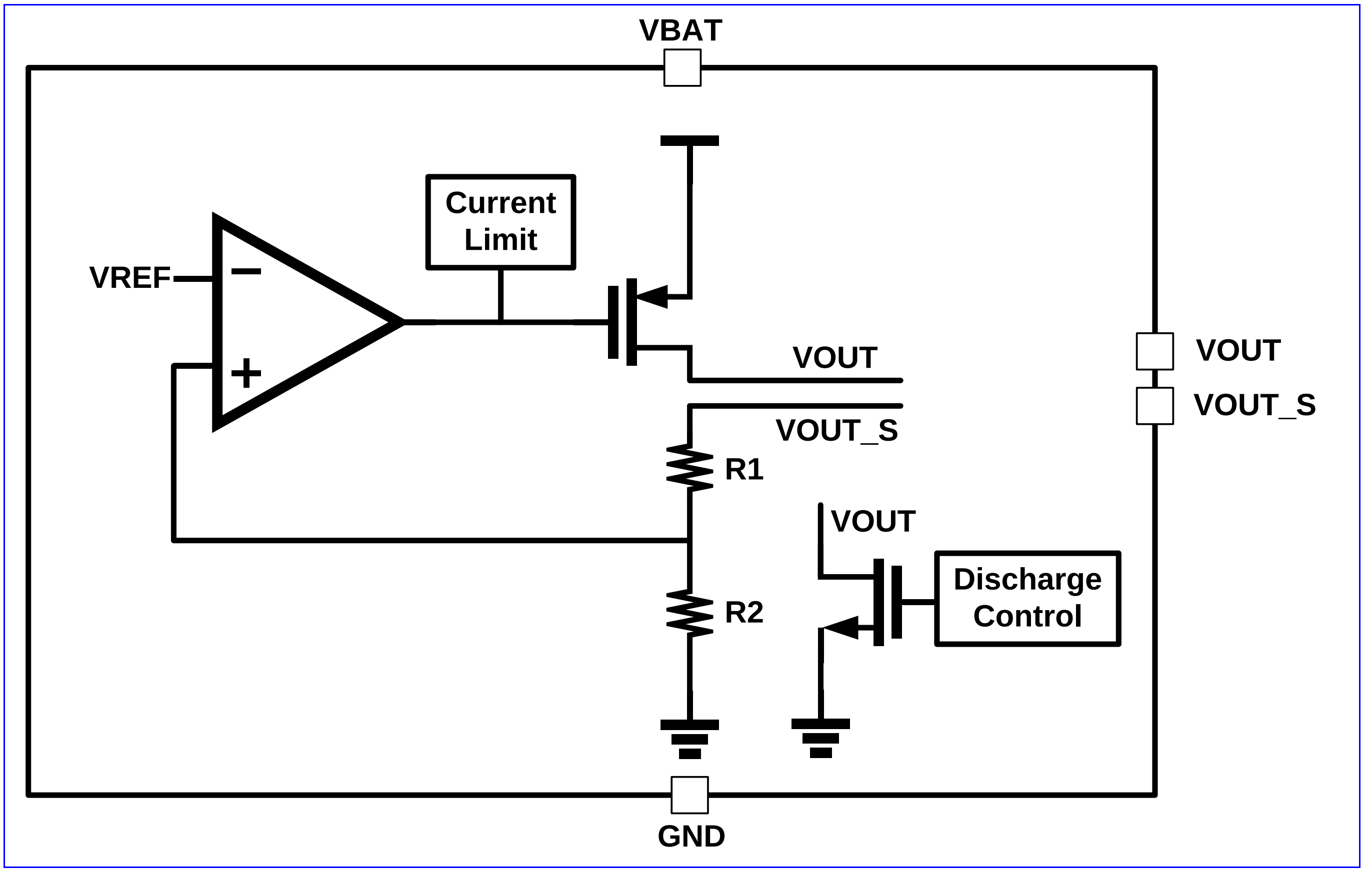


Figure 18 LDO block diagram

2.6.1.2 LDO Types

Type	LDO Name	Vout	Imax	Description
ALDO	VRF	2.85	200	RF chip
ALDO	VCAMA	1.5/1.8/2.5/2.8	250	Analog camera power
ALDO	VCAMA2	1.5/1.8/2.5/2.8	100	Analog camera power
ALDO	VTCXO	2.8	10	13/26 MHz reference clock
DLDO	VTV	2.8	45	TV DAC power
DLDO	VA25	2.5	30	Analog baseband

Type	LDO Name	Vout	Imax	Description
DLDO	VA12	1.25	30	Analog baseband
DLDO	VA25MIC	2.5	5	MIC interface power
DLDO	VAUDP	1.25	85	Audio head phone positive power
DLDO	VAUDN	-1.25	85	Audio head phone negative power
DLDO	VCAMD	1.3/1.5/1.8/2.5 2.8/3.0/3.3	100	Digital camera power
DLDO	VCAMD2	1.3/1.5/1.8/2.5 2.8/3.0/3.3	100	Digital camera power
DLDO	VM12	1.24	200	External Memory
DLDO	VM12_INT	1.35	50	Internal memory
DLDO	VIO28	2.8	100	Digital IO
DLDO	VSIM	1.8/3.0	100	SIM card
DLDO	VSIM2	1.3/1.5/1.8/2.5 2.8/3.0/3.3	100	SIM card
DLDO	VUSB	3.3	100	USB
DLDO	VMC	1.3/1.5/1.8/2.5 2.8/3.0/3.3	200	Memory card
DLDO	VIBR	1.3/1.5/1.8/2.5 2.8/3.0/3.3	200	Vibrator
DLDO	VRTC	2.8	2	Real-time clock

Table 31 LDO Types and Brief Specification

2.6.1.3 Functional Specification

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Load capacitor			1	2.2	μF
	Current limit		1.2*Imax		5*Imax	mA
	Vout	Include load regulation, line regulation, and temperature coefficient	max(-5%, -0.1V)		max(+5%, +0.1V)	V
	Transient response	Slew: 15mA/us	max(-5%, -0.1V)		max(+5%, +0.1V)	V
	Temperature coefficient			100		ppm/C

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	PSRR	Iout<0.5*Imax 217<f<3K Hz	65			dB
		Iout<0.5*Imax 3K<f<30K Hz	45			dB
	Output noise	10 to 80K Hz		90		uVrms
	Quiescent current	Iout=0			55	µA
	Turn-on overshoot	Iout=0			max(+10 %, +0.1V)	V
	Turn-on settling time	Iout=0			240./360	µF

Table 32 Analog LDO Specification

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Load capacitor			1	2.2	µF
	Current limit		1.2*Imax		5*Imax	mA
	Vout	Include load regulation, line regulation, and temperature coefficient	max(-5%, -0.1V)		max(+5% , +0.1V)	V
	Transient response	Slew: 15mA/us	max(-5%, -0.1V)		max(+5% , +0.1V)	V
	Temperature coefficient			100		ppm/C
	PSRR	Iout<0.5*Imax f=217Hz	40			dB
	Output noise	10 to 80K Hz		250	500	uVrms
	Quiescent current	Iout=0			15	µA
	Turn-on overshoot	Iout=0			max(+10 %, +0.1V)	V
	Turn-on settling time	Iout=0			360	µs

Table 33 Digital LDO Specification

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Load capacitor			0.1		µF
	Vout	Include load regulation, line regulation, and temperature coefficient	2	2.8	3	V
	Temperature coefficient				100	ppm/C
	Quiescent current	Iout=0		2		µA

Table 334 RTC LDO Specification

2.6.2 Buck Converter

2.6.2.1 Block Description

A BUCK is a step-down DC-DC converter which is capable of maintaining low power dissipation during input to output voltage conversion.

A BUCK consists of a reference, an error amplifier, a feedback voltage divider, comparators, power MOSFETs, slope compensation and PWM/PFM mode controller. A BUCK uses the fixed-frequency, peak current-mode PWM control architecture at medium to high loads, but shifts to a PFM mode control scheme at light loads to reduce the switching power losses and improve efficiency. When the devices operate in fixed-frequency PWM mode, output regulation is achieved by controlling the duty cycle of the integrated MOSFET. When the devices operate in PFM mode, the output voltage is controlled in a hysteretic manner with higher output ripple. In this mode of operation, the regulator periodically stops switching for a few cycles, thus keeping the conversion losses minimal to improve efficiency.

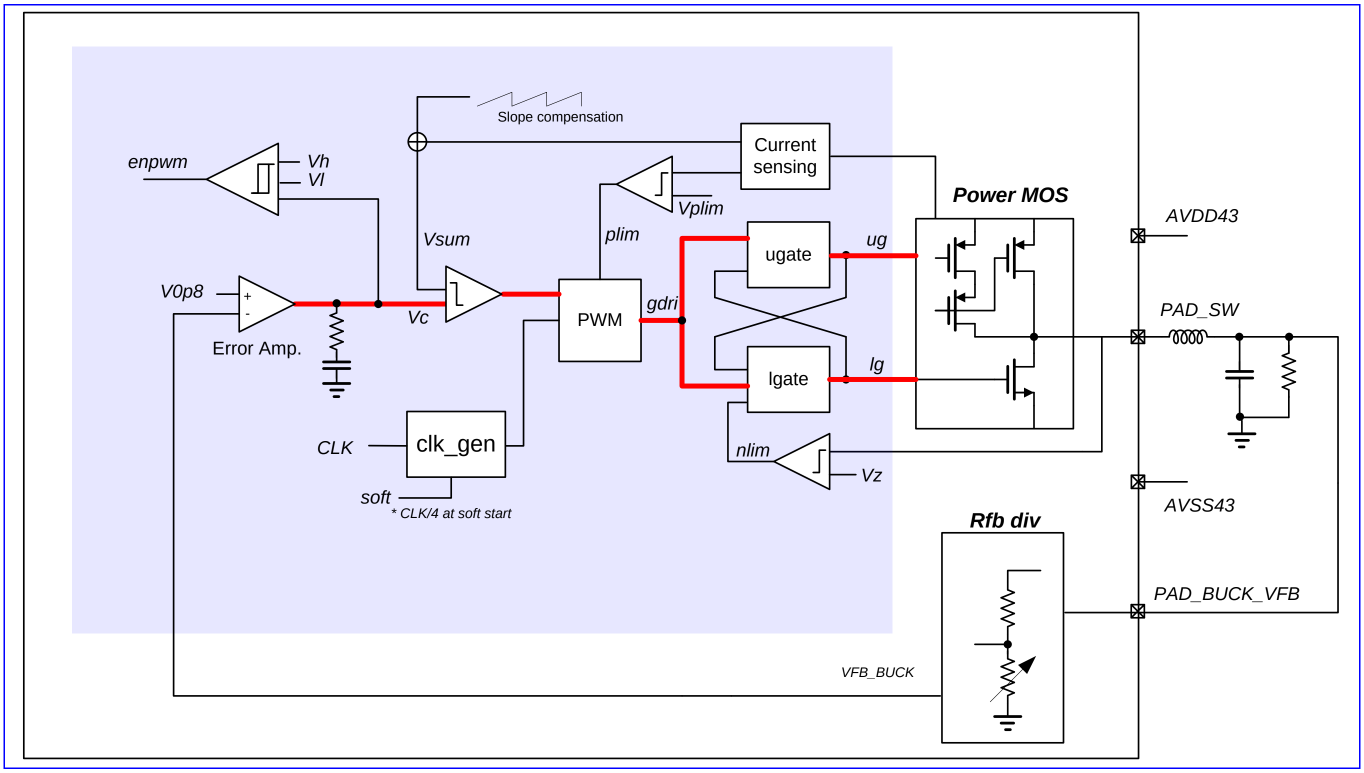


Figure 19 BUCK block diagram

2.6.2.2 Functional Specification (TBD)

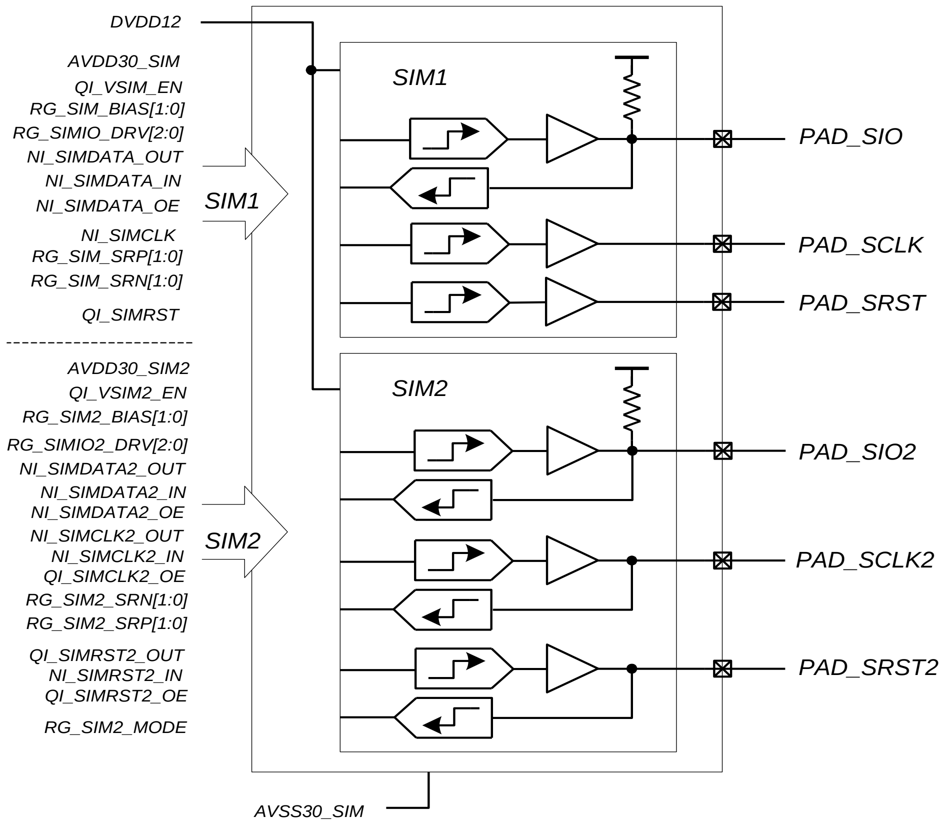
Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Maximum load current VCORE VPROC VIO18 VRF18 VPA		 - - - -	 - - - -	 600 600 600 250 800	 mA mA mA mA
	PFM/PWM threshold			50		mA
	Output Range VCORE VPROC VIO18 VRF18 VPA		 0.9 0.9 1.5	 1.8 1.8 	 1.375 1.45 3.4	 V V V V V
	Voltage error		-5		5	%
	Temperature Coefficient			100		ppm/deg
	Line regulation			1		%/V
	Load regulation			0.025		mV/mA
	Output ripple, constant load	Iload=Imax, Load Capacitor=4.7uF(ESR<30mohm)		15		mVpp
	Load transient response	Iload=1→Imax, slew rate=15mA/us		+/-5		%
	Efficiency	Inductance change within +/-10%, DCR<0.2 ohm		75		%

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Ground current			40		uA
	External components					
	Input capacitor			4.7		uF
	Output capacitor			4.7		uF
	Output capacitor (VPA)				4.7	uF
	Output inductor			2.2		uH
	Output inductor (VPA)			4.7		uH

Table 35

2.6.3 SIM Interface

2.6.3.1 Block Description



RG_SIM_BIAS[1:0] RG_SIM2_BIAS[1:0]	Slew rate
00	1×
01	1.25×
10	1.5×
11	2×

RG_SIMIO(2)_DRV[2] pull-up resistor enable 0: enable, 1: disable
RG_SIMIO(2)_DRV[1:0] pull-up resistor select

RG_SIMIO(2)_DRV[2:0]	pull-up resistor
000	5k
001	5k||10k
010	20k
011	20k||10k
1跂	disable

Figure 20 SIM interface block diagram

There are two SIM card interface modules to support two SIM cards simultaneously. The SIM card interface circuitry of PMU meets all ETSI and IMT-2000 SIM interface requirements. It provides level shifting needs for low voltage GSM controller to communicate with either 1.8V or 3V SIM cards. All SIM cards contain a clock input, a reset input, and a

bi-directional data input/output. The clock and reset inputs to SIM cards are level shifted from the supply of digital IO (Vio) of baseband to the SIM supply (Vsim). The bi-directional data bus is internal pull high to Vsim via 5KΩ resistor.

The 2nd SIM card interface can be used for supporting another SIM card or mobile TV. The interface pins such as SIO2, SRST2, SCLK2, can be configured as GPIO when there is no need to use the 2nd SIM card interface.

All pins that connect to the SIM card (Vsim, SRST, SCLK, SIO) withstand over 5kV HBM (human body mode) ESD. In order to ensure proper ESD protection, careful board layout is required.

2.6.3.2 Functional Specification

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Interface to 3 V SIM Card						
	Output Low of SRST	I = 200 µA			0.36	V
	Output High of SRST	I = -200 µA	0.9*VSIM			V
	Output Low of SCLK	I = 200 µA			0.4	V
	Output High of SCLK	I =-100 µA	0.9*VSIM			V
	Input/Output Low of SIO	I=-1mA			0.4	V
	Input/Output High of SIO	I = ±20 µA	VSIM-0.4			V
	(Iil)Pull high current of SIO	Vil = 0 V			-1	mA
	(Vol)Input/Output Low of SIO	Iol = 1 mA			0.4	V
Interface to 1.8 V SIM Card						
	Output Low of SRST	I = 200 µA			0.2*VSIM	V
	Output High of SRST	I = -200 µA	0.9*VSIM			V
	Output Low of SCLK	I = 200 µA			0.12*VSIM	V
	Output High of SCLK	I = -100 µA	0.9*VSIM			V
	Input/Output Low of SIO	I=-1mA			0.15*VSIM	V
	Input/Output High of SIO	I = ±20 µA	VSIM-0.4			V
	(Iil)Pull high current of SIO	Vil = 0 V			-1	mA
	(Vol)Input/Output Low of SIO	Iol = 1 mA			0.15*VSIM	V
SIM Card Interface Timing						
	SIO pull-up resistance to VSIM		4	5	6	kΩ
	SRST, SIO rise/fall times	VSIM = 3, 1.8 V, load with 30 pF			1	µs
	SCLK rise/fall times	VSIM = 3 V, CLK load with 30 pF			18	ns
		VSIM = 1.8 V, CLK load with 30 pF			50	ns
	SCLK frequency	CLK load with 30 pF			5	MHz
	SCLK duty cycle	SIMCLK Duty = 50%, fsimclk = 5 MHz	47		53	%

Table 36

2.6.4 Keypad LED Switches

2.6.4.1 Block Description

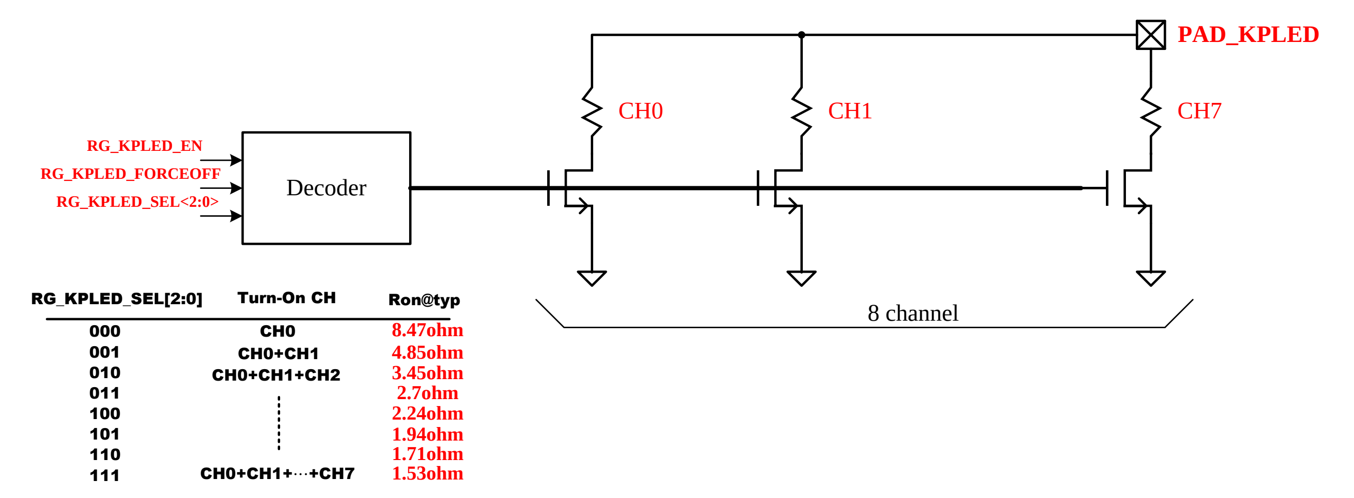


Figure 21 Vibrator and Keypad LED block diagram (TBD)

Driver	Type	Current	Description
KPLED	Open-drain NMOS switch	>150 mA	Drives the keypad LEDs

Table 37

2.6.4.2 Functional Specification

The Keypad LED connects its anode to VBAT and its cathode to the ballast resistor. The other terminal of the ballast resistor connects to the driver of MT6573. The Keypad LED driver is a low Ron switch which allows 150mA current.

The brightness of the Keypad LED can be controlled by changing the external ballast resistor or switching on/off the driver through dimming control. The dimming frequency and duty can be programmed by registers through I2C interface. For the details, please refer to the “dimming control” section.

2.6.5 Battery Charge

2.6.5.1 Block Description

The charger circuit in MT6573 is shown as follows.

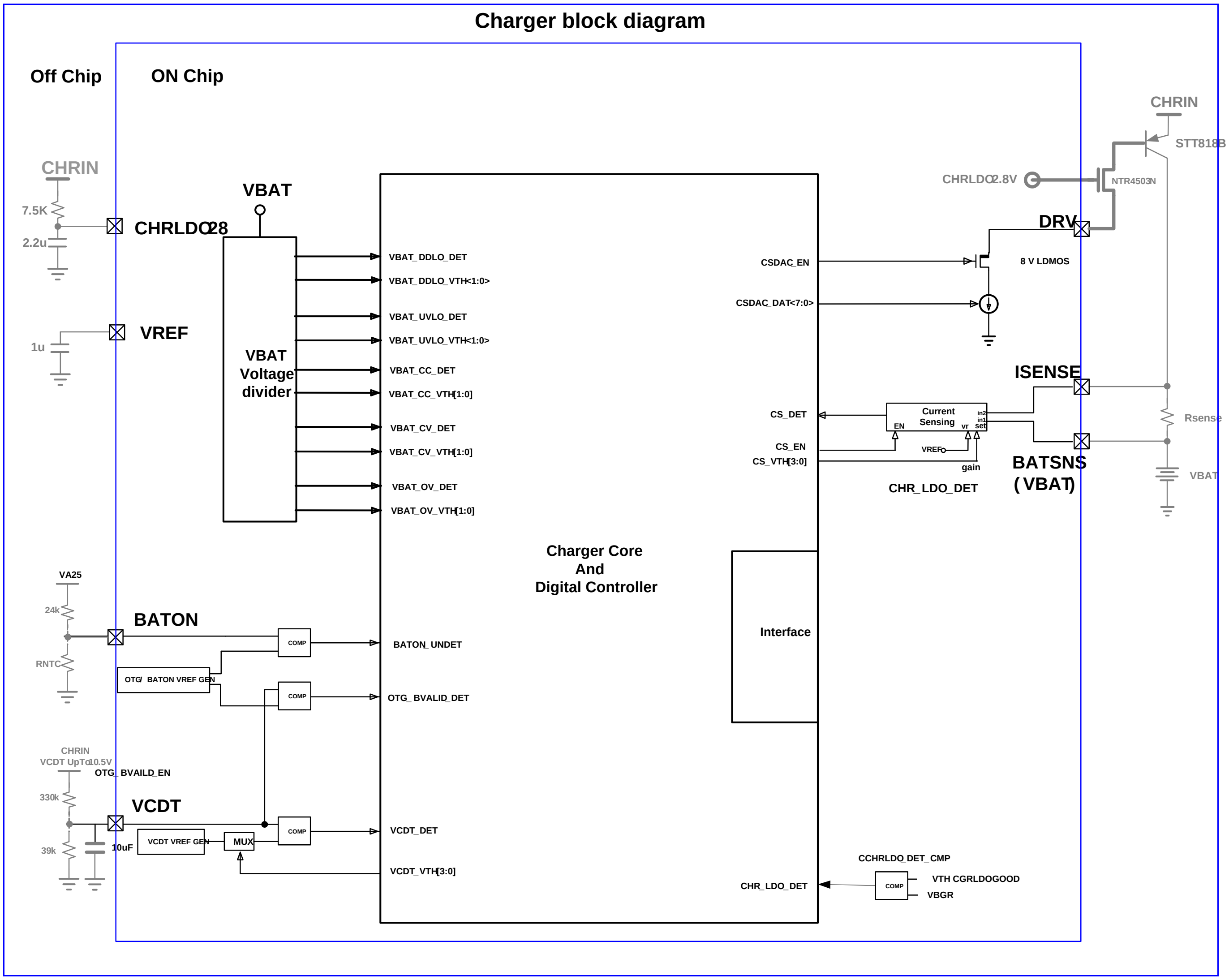


Figure 22 Battery charger block diagram

2.6.5.2 Functional Specification

The charger controller senses the charger input voltage (CHRIN) from either a standard AC-DC adaptor or an USB charger. When the charger input voltage is within a pre-determined range, the charging process is activated. This detector can resist higher input voltages than other parts of the PMIC. Therefore, if an invalid charging source is detected (> 7.0 V), the charger detector stops the charging process immediately to avoid burning out the chip or even the phone.

2.6.5.3 Charging Control

When the charger is active, the charger controller manages the charging phase according to the battery status. During the charging period, the battery voltage is constantly monitored. The battery charger in MT6573 supports pre-charge mode (VBAT<3.2V, switched-off state), CC mode (constant current mode or fast charging mode at the range of 3.2V<VBAT<4.2V) and CV mode (constant voltage mode) to optimize the charging procedure for Li-ion battery.

2.6.5.3.1 Pre-charge Mode

When the battery voltage is in the UV state, the charger operates in the pre-charge mode. There are two steps in this mode. While the battery voltage is deeply discharged below 2.2V, a IPRECC0 trickle charging current applies to the battery. When the battery voltage exceeds 2.2V, the closed-loop pre-charge is enabled. The voltage drop across the external Rsense is kept around 25mV (Typ.). The closed-loop pre-charge current can be calculated:

$$I_{PRE_CHARGING} = \frac{V_{SENSE}}{Rsense} = \frac{25mV}{Rsense}$$

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	IPRECC0	VBAT<2.2V	30	50	80	mA
	Pre-charging current	VBAT<2.2V	5	10	30	mA
		VBAT>=2.2V	$12/R_{sense}$	$20/R_{sense}$	$36/R_{sense}$	mA
	Pre-charging indicator current	Pre-charging		5		mA
	Pre-charging off threshold	CHR_EN=L		3.3		V
	Pre-charging off hysteresis			0.4		V

Table 38 Pre-charge Specifications

2.6.5.3.2 Constant Current Mode

As the battery is charged up and over 3.2V, it can switch to the CC mode. (CHREN should be high) In CC mode, several charging currents can be set by programming registers or the external Rsense resistor. The charging current can be determined by Vch,ref/Rsense, where Vch,ref is programmed by registers. For example, if Rsense is selected as 0.2Ohm, the CC mode charging current can be set from 50mA to 800mA. It can accommodate the battery charger to the various charger inputs with different current capability.

Due to process variation, the charging current may vary form chip to chip. To compensate for this variation, the offset registers can be set in MT6573. The PMIC reads this compensation value and applied the charging current offset when the phone is in the charging state. This compensation value could be obtained during the calibration process in phone production, or it could be constantly observed by the BB while the phone is charging.

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	CC mode charging current	CHR_CC_LEVEL [2:0]=000		$14/R_{sense}$		mA
		CHR_CC_LEVEL [2:0]=001		$40/R_{sense}$		mA
		CHR_CC_LEVEL [2:0]=010		$80/R_{sense}$		mA
		CHR_CC_LEVEL [2:0]=011		$90/R_{sense}$		mA
		CHR_CC_LEVEL [2:0]=100		$110/R_{sense}$		mA
		CHR_CC_LEVEL [2:0]=101		$130/R_{sense}$		mA
		CHR_CC_LEVEL [2:0]=110		$140/R_{sense}$		mA
		CHR_CC_LEVEL [2:0]=111		$160/R_{sense}$		mA

Table 39 Constant Current Specifications

Note: SA should help to judge (1). which spec. items are required for our customers, (2). testing condition of each spec. items, and (3). which items should not release to our customers.

2.6.5.3.3 Constant Voltage Mode and Protection

If the battery voltage has reached the final value, said 4.2V, a constant voltage is applied to the battery and keeps it at 4.2V. After that, the charging current becomes smaller and smaller. When the charging current is less than a pre-determined threshold for a while, it enters the charge complete state. The charging process will be terminated by setting CHREN=0. The charge complete detection and CHREN control are managed by BB/SW.

Once the battery voltage exceeds 4.3V for any reason, the hardware over voltage protection (OV) will take action and turn off the charger immediately to prevent permanent damage to the battery.

When charging, the PMIC uses GATEDRV pin to control the current flow through the base of the external BJT. The charging current from the collect BJT of is sensed by the voltage drop across the external Rsense resistor (Typ. 0.2 Ω). Then the charging controller and the external components (NMOS,BJT, Rsense and battery) form a regulated charging loop.

During charging, the battery removal might cause the VBAT voltage to surge, damaging the chip before the over-voltage protection is enabled. Pin BAT_ON turns off the charger immediately if it goes high (> 2.205±0.1 V). This function is designated to stop CC or CV charging mode in case the battery is accidentally removed.

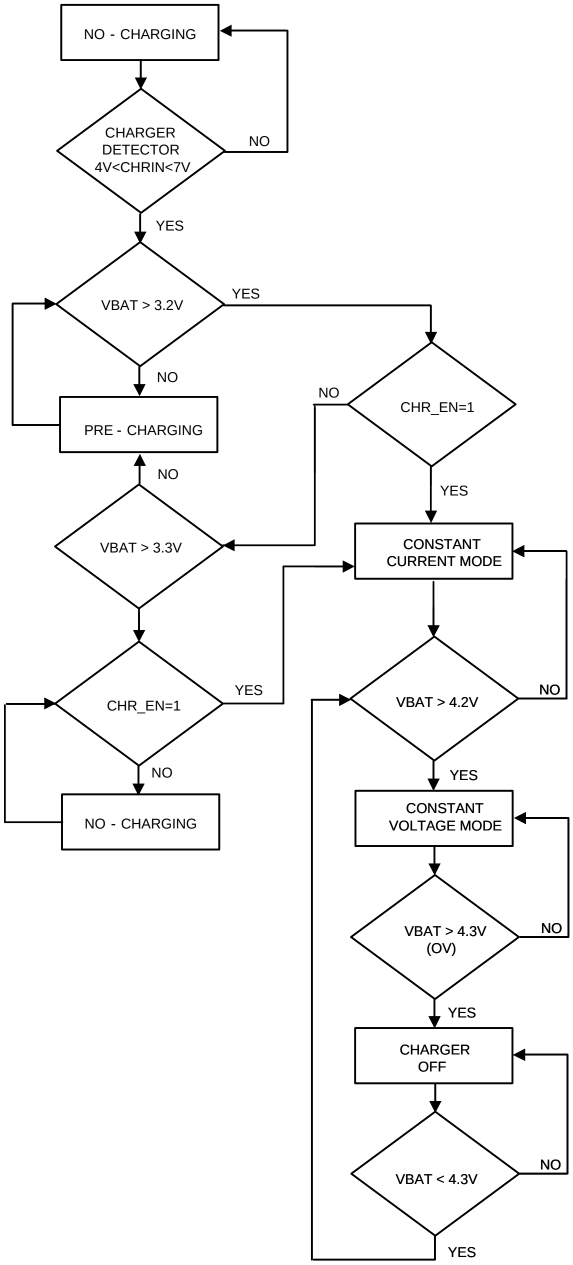
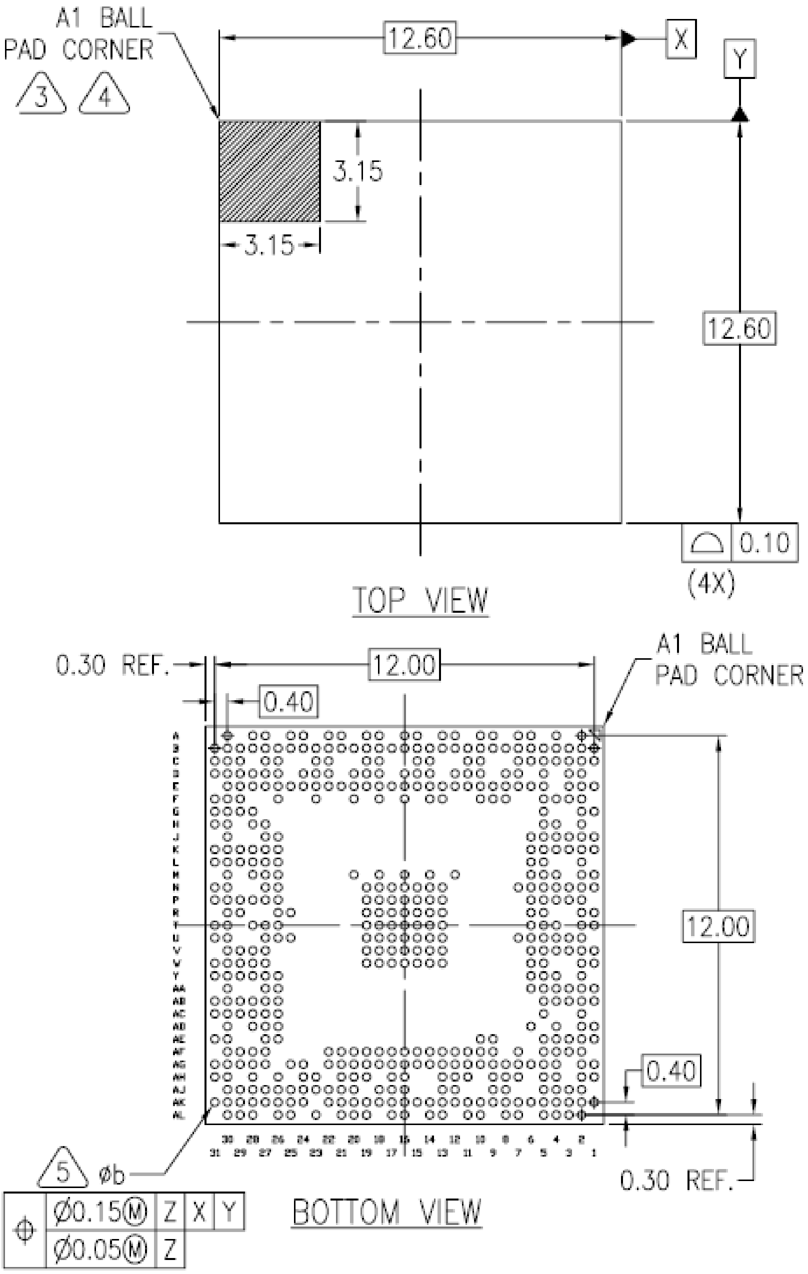


Figure 23 Charging States Diagram

2.7 Package Information

2.7.1 Package Outlines



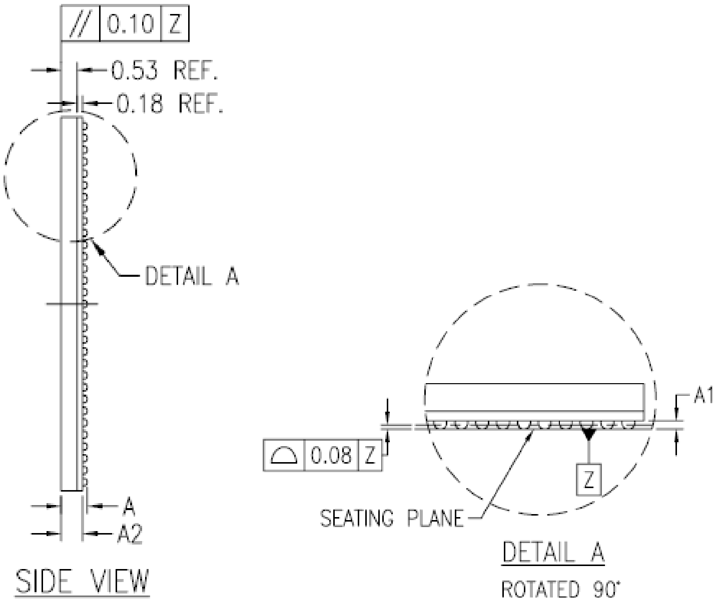


Figure 24 Outlines and Dimension of TFBGA 12.6mm*12.6mm, 518-ball, 0.4 mm pitch Package

2.7.2 Thermal Operating Specifications

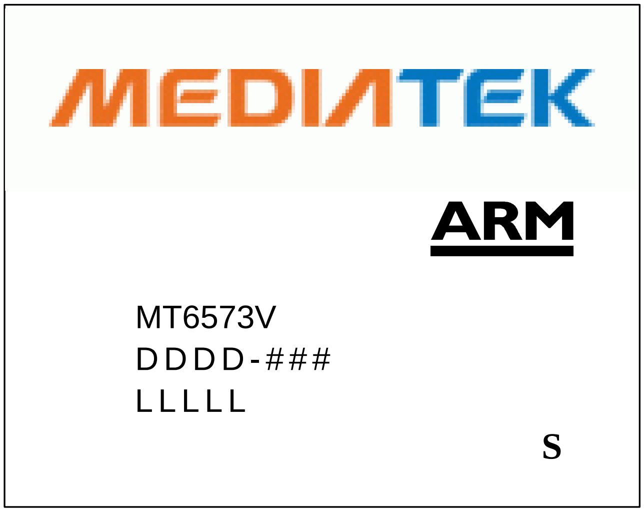
Symbol	Description	Value	Unit	Notes
	Thermal resistance from device junction to package case	125	°C	
	Maximum Package Temperature	80	°C	
	Maximum power dissipation	1.86	Watt	

2.7.3 Lead-free Packaging

The MT6573 is provided in a lead-free package and can meet RoHS requirements

2.8 Ordering Information

2.8.1 Top Marking Definition



MTXXXXXX	Part No.
DDDD:	Date Code
###:	Subcontractor Code
LLLLL:	Die Lot No.
S:	Special Code

Figure 25 Top Mark of MT6573